June 2011
Version 1.0

AR8327/AR8327N Seven-port Gigabit Ethernet Switch

General Description

The AR8327 is a highly integrated seven-port Gigabit Ethernet switch with non-blocking switch fabric, a high-performance lookup unit with 2048 MAC address, and a four-traffic class Quality of Service (QoS) engine. The AR8327 has the flexibility to support various networking applications. The AR8327 is designed for cost-sensitive switch applications in wireless AP routers, home gateways, and xDSL/cable modem platforms.

The AR8327 integrates all the functions of a high-speed Switch system, including packet buffer, PHY transceivers, media access controllers, address management, and a non-blocking switch fabric into a single 0.11 um CMOS device. It complies with 10BASE-Te, 100BASE-Tx & 1000BASE-T specifications, including the MAC control, pause frame, and auto-negotiation subsections, providing compatibility with all industry-standard Ethernet, Fast Ethernet & Gigabit Ethernet networks.

The AR8327 device contains five full-duplex 10BASE-Te/100BASE-TX/1000BASE-T transceivers and 10BASE-Te/100BASE-TX can run at half duplex, each of which performs all of the physical layer interface functions for 10BASE-Te Ethernet on Category 5 unshielded twisted-pair (UTP) cable and 100BASE-TX Fast/Gigabit Ethernet on Category 5 UTP cable. The remaining 2 ports feature a standard GMII/RGMII/MII/Serdes interface to allow connection to a host CPU in PON/xDSL/Cable/Wifi/Fiber routers. The media access controllers on the AR8327 also support Jumbo Frames which are typically used for high-performance connections to servers because they offer a smaller percentage of overhead on the link for more efficiency.

MDC/MDIO or EEPROM interfaces provide easy programming of the on-chip 802.1p QoS and/or DiffServ/TOS. This allows switch traffic to be given different classes of priority or service - for example, voice traffic for IP phone applications, video traffic for multimedia applications, or data traffic for e-mail. Up to 4K Virtual LANs (VLANs) can be set up via the MDC/MDIO port for separation of different users or groups on the network. ACL features can reduce CPU effort for VLAN/Q.O.S/DSCP/Forward mapping & remapping based on layer1 to Layer4 information. 16 PPPoE header add/removal can increase Video quality and offload the CPU. Hardware IGMP V1/V2/V3 is an innovation for IPTV service. Green Power can increase energy efficiency for no link or idle states.

The AR8327N chip supports hardware NAT (Network Address Translation) to offload the CPU and achieve the full wire speed when doing NAT. The AR8327/AR8327N supports the following modes of NAT.

1. Basic NAT: This involves IP address translation only, not port mapping.
2. Network Address Port Translation (NAPT): This involves the translation of both IP addresses and port numbers. For the NAPT mode, the AR8327/AR8327N can support Full cone NAT, Restricted cone NAT, Port-Restricted cone NAT and Symmetric NAT.

e AR8327/AR8327N supports the following configurations

- 5*10/100/1000Base-T + GMII/RGMII/MII + 1* Serdes
- 5* 10/100/1000Base-T + 2*RGMII/MII
- 4* 10/100/1000Base-T + 1*RGMII/MII + 1* Single RGMII PHY

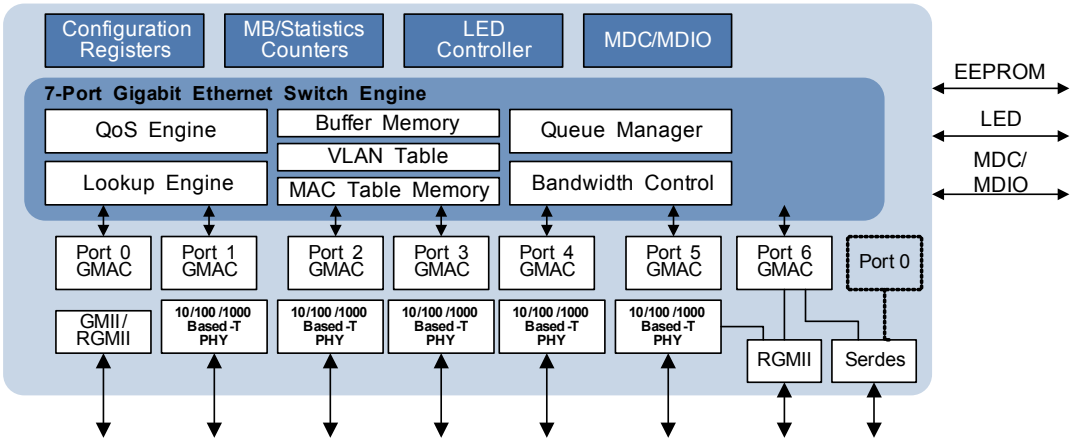
AR8327/AR8327N Features

The AR8327 chip family includes a 7-port MAC structure to support the following family of switch chips:

- Supports 802.3az Power Management
- The AR8327N chip includes the Hardware NAT (Network Address Translation) function

- The AR8327 chip (without the 'N' designation) does not contain the Hardware NAT function
- ACL Mask Rule from Layer1~4. Port No, DA, SA, Ethernet Type, VLAN, IP Protocol, IPv4/v6 Source/Destination Address, TCP/UDP Source/Destination port
- 96 ACL Mask Rule for Pass/Drop, VLAN/ Q.O.S./DSCP Mapping/Translation
- User define ACL up to 48 bytes depth in Layer 4/3/2
- Q.O.S mechanisms include Weight Round Robin, Strict, Hybrid Up Queue
- Port Base VLAN & 4K 802.1Q VLAN Group
- IVL & SVL
- IGMP Snooping V1, V2 & V3. IPv6 MLD V1/ V2 forwarded to CPU
- Supports Light Hardware IGMP snooping v1/v2/v3, MLDv1/v2 and Smart Leave
- Hardware Looping Detection
- QinQ function for SVLAN & CVLAN Translation
- IP Packet/PPPoE bypass to reduce CPU loading on Video packet
- 16 PPPoE session support/PPP Session Header Removal/Addition
- Scalable Ingress/Egress Bandwidth Control
- 40 MIBs Counter/Port & Port Status.
- 1M Bit Packet Buffer
- Supports 9K Jumbo Frame
- Port Mirror, 802.1X Security, Rapid Spanning Tree
- Rule-based Bandwidth Control
- Programmable Wake on LAN
- Half Power Mode for Cable length less than 30m (for home installations)
- Supports Internal/External Loopback
- Supports Reduced AFE circuit
- 2K MAC Table. Edit, Search, Add & Delete.
- MAC Limit by Port/Chip/VLAN
- Trunking Function
- Supports Trunking and auto-failover
- Power Saving on Cable no Link, short Cable & 10BASE-Te Idle
- Supports 1K NAPT entries and 128 hardware based host routing (ARP) entries
- Supports hardware-based IP source guard, ARP inspection, routing/L3 switching
- Supports VLAN translation and mapping with 64 Translation entries
- 148 pin DRQFN, 0.11um

AR8327 System Block Diagram



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Revision History

Table 0-1. **AR8161-A Revision History**

Date	Revision Details	Revision
2011/2/24	First draft	0.31
2011/6/10	General ■ Typo and grammar corrections ■ Reference corrections Pin Description ■ Update drawing to re-organize inner(B) and outer (A) pins ■ Table 1-1: change A54 pin type to I/O, PU Function Descriptions ■ Table 2-34 and 2-35: change PRIVATE_IP_ADDR_MODE to PRIVATE_IP_BASE_SEL ■ 2.7.2 Action Definition: add description ■ 2.21 Memory Map: update memory map Registers ■ 3.2.2 PORT0 PAD MODE CTRL, update bit[18] bit[19] definitions ■ 3.2.3 PORT5 PAD MODE CTRL (0x0008): add description for bit[10] ■ 3.2.5 PWS_REG (0x0010): update bit definitions ■ 3.5.22 to 3.5.24 IPv6 Private Base Address Register 0-2: new registers ■ 3.8.12 to 3.8.14 Router Default VID Register 0-2: new registers ■ 3.8.16 Router Egress VLAN Mode (0x0C80): new register ■ 3.10.24 Debug Port 2 (0xIE): change decimal address to “0d30“ ■ 3.10.25 Debug Register—Analog Test Control (0x00): new register ■ 3.10.26 Debug Register—System Mode Control (0x03): new register ■ 3.10.28 Debug Register—Hib Control and Auto Negotiation Test Register (0x0B): new register ■ 3.10.30 Debug Register—Green Feature Configure Register (0x3D): new register ■ 3.13 MMD7—Auto-negotiation Register: update bit definitions ■ 3.13.3 to 3.13.7: update decimal address ■ 4.6 Typical Power Consumption Parameters: update “two ports active” and “three ports active“ values Package Dimensions ■ Update package illustration Ordering ■ Update ordering method for tape&reel and tray Top Side Marking ■ Add package top marking illustration	1

1. Pin Descriptions

This section contains a listing of the signal descriptions (see Table 1-1 and Figure 1-1 through Figure 1-2).

The following nomenclature is used for signal names:

_L	At the end of the signal name, indicates active low signals
N	At the end of the signal name indicates the negative side of a differential signal
NC	No connection should be made to this pin
P	At the end of the signal name, indicates the positive side of a differential signal

The following nomenclature is used for signal types described in Table 1-1:

D	Open drain for digital pads
I	Digital input signal
I/O	Digital bidirectional signal
IA	Analog input signal
IH	Digital input with hysteresis
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
O	Digital output signal
OA	Analog output signal
P	A power or ground signal
PD	Internal pull-down for digital input
PU	Internal pull-up for digital input

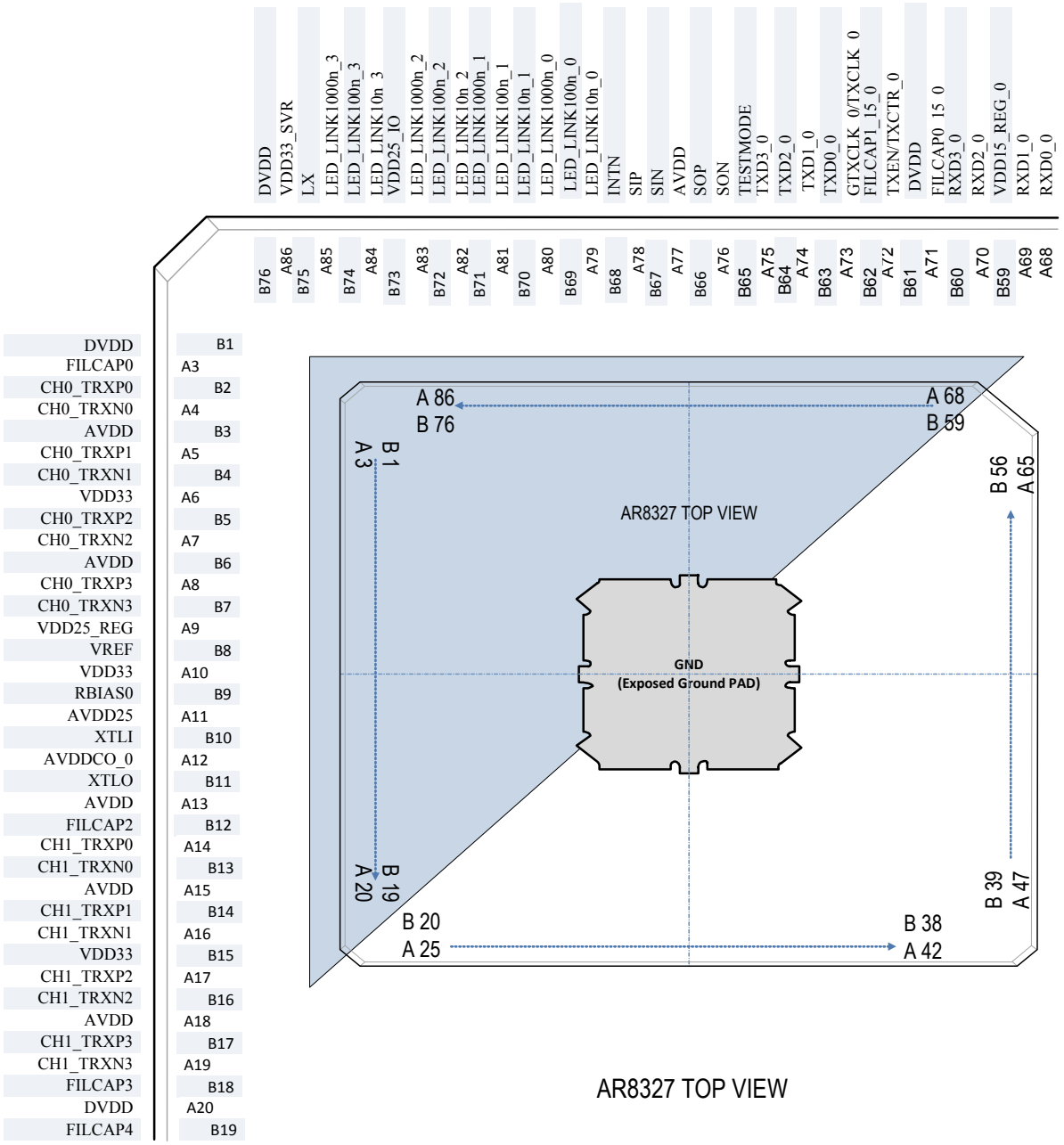


Figure 1-1. **148 Pin DRQFN Package Pinout (Part 1)**

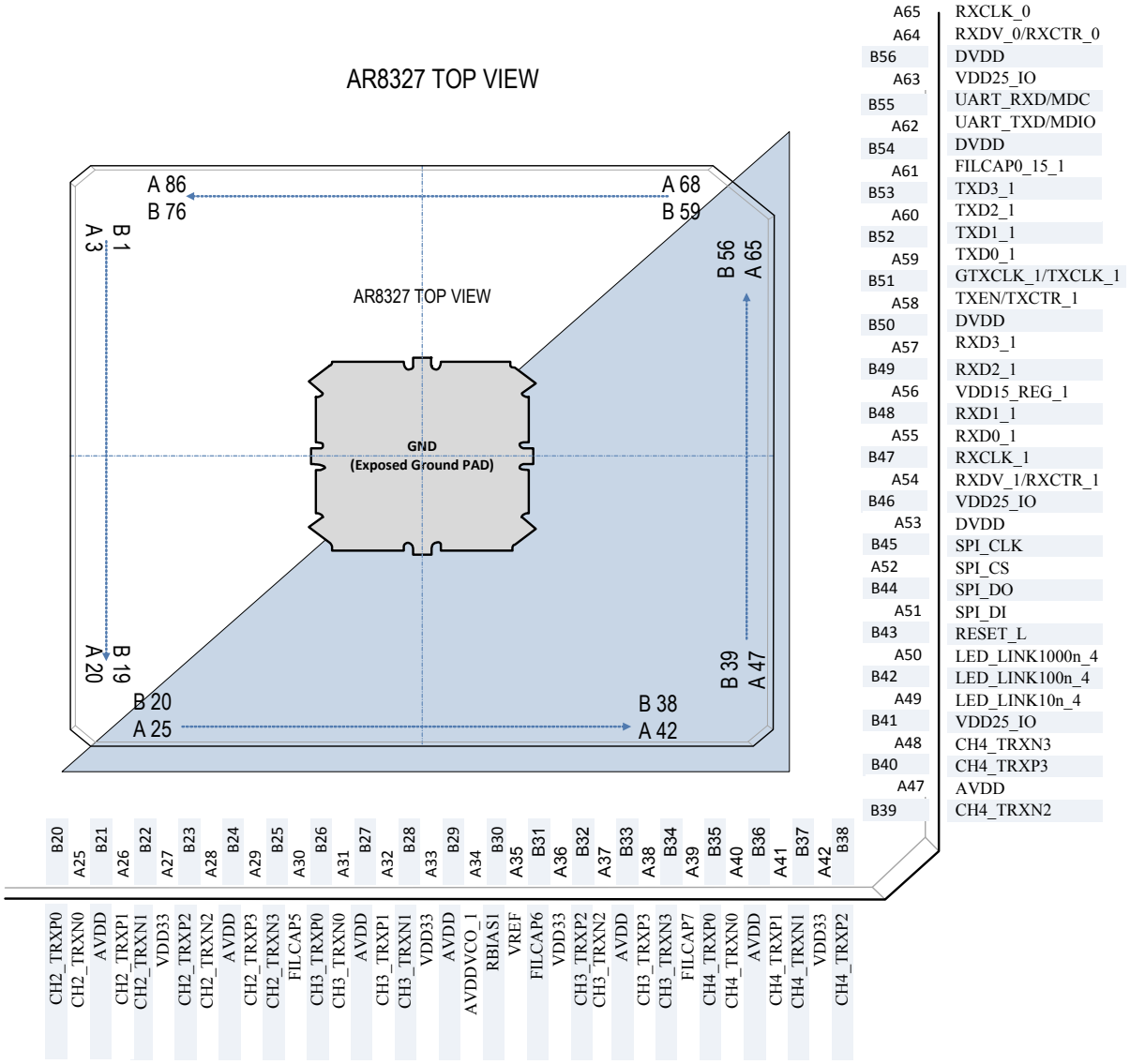


Figure 1-2. **148 Pin DRQFN Package Pinout (Part 2)**

Table 1-1. **Signal to Pin Relationships and Descriptions**

Symbol	Pin	Type	Description
Media Connection			
CH0_TRXN0	A4	IA, OA	Media-dependent interface, MDI[3:0]: Transmitter output positive/negative
CH0_TRXP0	B2		
CH0_TRXN1	B4	IA, OA	Connect derectly to Transformer without any pull-down terminators, such as resistors or capacitors, required.
CH0_TRXP1	A5		
CH0_TRXN2	A7	IA, OA	
CH0_TRXP2	B5		
CH0_TRXN3	B7	IA, OA	
CH0_TRXP3	A8		
CH1_TRXN0	B13	IA, OA	Media-dependent interface, MDI[3:0]: Transmitter output positive/negative
CH1_TRXP0	A14		
CH1_TRXN1	A16	IA, OA	Connect derectly to Transformer without any pull-down terminators, such as resistors or capacitors, required.
CH1_TRXP1	B14		
CH1_TRXN2	B16	IA, OA	
CH1_TRXP2	A17		
CH1_TRXN3	A19	IA, OA	
CH1_TRXP3	B17		
CH2_TRXN0	A25	IA, OA	Media-dependent interface, MDI[3:0]: Transmitter output positive/negative
CH2_TRXP0	B20		
CH2_TRXN1	B22	IA, OA	Connect derectly to Transformer without any pull-down terminators, such as resistors or capacitors, required.
CH2_TRXP1	A26		
CH2_TRXN2	A28	IA, OA	
CH2_TRXP2	B23		
CH2_TRXN3	B25	IA, OA	
CH2_TRXP3	A29		
CH3_TRXN0	A31	IA, OA	Media-dependent interface, MDI[3:0]: Transmitter output positive/negative
CH3_TRXP0	B26		
CH3_TRXN1	B28	IA, OA	Connect derectly to XFMR without any pull-down terminators, such as resistors or capacitors, required.
CH3_TRXP1	A32		
CH3_TRXN2	A37	IA, OA	
CH3_TRXP2	B32		
CH3_TRXN3	B34	IA, OA	
CH3_TRXP3	A38		

Table 1-1. **Signal to Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
CH4_TRXN0	A40	IA, OA	Media-dependent interface, MDI[3:0]: Transmitter output positive/negative Connect directly to XFMR without any pull-down terminators, such as resistors or capacitors, required.
CH4_TRXP0	B35		
CH4_TRXN1	B37	IA, OA	
CH4_TRXP1	A41		
CH4_TRXN2	B39	IA, OA	
CH4_TRXP2	B38		
CH4_TRXN3	A48	IA, OA	
CH4_TRXP3	B40		
MAC 0/CPU port GMII/RGMII interface			
GTXCLK_0/TXCLK_0	A73	I/O, PU	RGMII transmit clock, 125 MHz/25 MHz, or configurable. This is the reference clock input for RGMII mode, PHY type interface, or MII mode MAC type interface. It also supports 50MHz clock input (Turbo-MII) when operating in MII mode, MAC type interface.
RXCLK_0	A65	I/O, PD	RGMII receive clock. This is output clock from MAC0 when AR8327 operates a PHY type interface. It can be 125MHz/ 25MHz/2.5MHz —depending upon the operating speed.
RXD0_0	A68	I/O, PD	RGMII/MII — receive data or configuration; recommend adding a 22 Ω damping resistor. these are output signals from MAC0. The RXD[3:0]_0 are used as data input when operating at RGMII or MII mode. The reference clock for these output signals will be: RXCLK_0 (pin A65): RGMII/MII PHY type interface and GMII-MAC type interface.
RXD1_0	A69	I/O, PD	
RXD2_0	A70	I/O, PD	
RXD3_0	B60	I/O, PD	
RXDV_0/RXCTR_0	A64	I/O, PD	RGMII/MII received data; valid. This is output signal for MAC0.
TXEN/TXCTR_0	A72	I, PD	RGMII/MII transmit enable, this is input signal for the MAC0.
TXD0_0	B63	I, PD	RGMII/MII transmit data, these are input signals for MAC0. All the data bits TXD[7:0]_0 are used in GMII mode. The TXD[3:0]_0 are used as data input when operating on RGMII or MII mode. The reference clock for these input signals will be: 1. GTXCLK_0 (pin A73): RGMII/MII mode 2. GTXCLK_0 (pin B51): GMII mode
TXD1_0	A74	I, PD	
TXD2_0	B64	I, PD	
TXD3_0	A75	I, PD	
MAC 6/PHY 4 RGMII/MII			
GTXCLK_1/TXCLK_1	B51	I/O, PD	RGMII transmit clock, 125 MHz/25 MHz, or configuration. This is the reference clock input for RGMII mode PHY type interface or MII mode MAC type interface.
RXCLK_1	B47	I/O, PD	RGMII receive clock. This is output clock from PHY 4 when the AR8327 operates a PHY type interface. It can be 125MHz/ 25MHz/2.5MHz depending on the operating speed.

Table 1-1. **Signal to Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
RXD0_1	A55	I/O, PD	RGMII receive data or configuration. These are output signals sourced from either PHY4. All the data bits RXD[7:0]_1 are used in GMII mode. The RXD[3:0]_1 are used as data input when operating in RGMII mode. The reference clock for these output signals will be: RXCLK_1 (pin B47): RGMII/MII PHY type interface and GMII MAC type interface.
RXD1_1	B48	I/O, PD	
RXD2_1	B49	I/O, PD	
RXD3_1	A57	I/O, PU	
RXDV_1/RXCTR_1	A54	I/O, PU	RGMII receive data valid. This is output signal for either or PHY4.
TXEN/TXCTR_1	A58	I, PD	RGMII transmit enable, this is an input signal for PHY4.
TXD0_1	A59	I, PD	RGMII transmit data, these are input signals for either PHY4. All the data bits TXD[7:0]_1 are used in GMII mode. The TXD[3:0]_1 are used as data input when operating in RGMII mode. The reference clock for these input signals: GTXCLK_1 (pin B51): RGMII PHY type interface
TXD1_1	B52	I, PD	
TXD2_1	A60	I, PD	
TXD3_1	B53	I, PD	
LED			
LED_LINK10n_0	A79	O, D	LED_LINK10n[4:0] Parallel LED output for 10 Base-T link/speed/activity, active low. The LED inactive state can be open-drain or driving high output, depending upon the power-on strapping setup. The LED behaviour can be configurable, see the LED Control Registers 0x0050 ~ 0x005C. 10n offset is 0x0058
LED_LINK10n_1	B70	O, D	
LED_LINK10n_2	A82	O, D	
LED_LINK10n_3	A84	O, D	
LED_LINK10n_4	A49	O, D	
LED_LINK100n_0	B69	O, D	LED_LINK100n[4:0] Parallel LED output for 100 Base-T link/speed/activity, active low. The LED inactive state can be open-drain or driving high output, depending on the power-on strapping. The LED behaviour can be configured, see the LED Control Registers 0x0050 ~ 0x005C. 100n offset is 0x0054
LED_LINK100n_1	A81	O, D	
LED_LINK100n_2	B72	O, D	
LED_LINK100n_3	B74	O, D	
LED_LINK100n_4	B42	O, D	
LED_LINK1000n_0	A80	O, D	LED_LINK1000n[4:0] Parallel LED output for 1000 Base-T link/speed/activity, active low. The LED inactive state can be open-drain or driving high output, depending upon the power-on strapping setup. The LED behaviour can be configured, see the LED Control Registers 0x0050 ~ 0x005C. 1000n offset is 0x0050
LED_LINK1000n_1	B71	O, D	
LED_LINK1000n_2	A83	O, D	
LED_LINK1000n_3	A85	O, D	
LED_LINK1000n_4	A50	O, D	
UART/MDIO and SPI EEPROM			
SPI_CLK	B45	I/O, PD	SPI Clock or configuration
SPI_CS	A52	I/O, PD	SPI Chip select configuration
SPI_DI	A51	I, PD	SPI Data input
SPI_DO	B44	I/O, PU	SPI Data out or configuration
UART_RXD/MDC	B55	I, PU	Management data clock reference
UART_TXD/MDIO	A62	I/O	Management data
Serdes Interface			
SOP	B66	OA	Serdes differential output pair

Table 1-1. **Signal to Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description	
SON	A76	OA	Serdes differential output pair	
SIP	A78	IA	Serdes differential input pair	
SIN	B67	IA	Serdes differential input pair	
Miscellaneous				
RBIAS	B9, B30	OA	Connect 2.37 kΩ resistor to GND. The resistor value is adjustable, depending on the PCB.	
RESET_L	B43	IH	Chip reset, active low. The active low duration must be greater than 10ms.	
TESTMODE	B65	I	0	Normal mode
			1	Test mode
XTLI	B10	IA	Crystal oscillator input, connect a 27 pF capacitor to GND. An external 25 MHz clock with swing from 0–1 V can be injected to this pin. When an external clock source is used, the 27 pF capacitor should be removed from this pin and the 27 pF capacitor at XTLO should be maintained.	
XTLO	B11	OA	Crystal oscillator output, connect a 27 pF capacitor to GND	
INT_n	B68	I/O, PU	Interrupt, active low. see the global interrupt register for detail	
VREF	B8, A35	OA	Reference voltage, put a 1 nF cap to GND	

Symbol	Pin	Type	Description
Power			
AVDD	B3, B6, A13, A15, A18, B21, B24, B27, B29, B33, B36, A47, A77	P	Analog 1.1V power input
DVDD	B1, A20, A53, B50, B54, B56, B61, B76	P	Digital 1.1V power input
VDD15_REG_0	B59		MAC 0 interface power source. It can be connected to external 2.5V power or only connect an external capacitor 1uF and using internal LDO for 1.8V or 1.5V interface power.
VDD15_REG_1	A56	P	MAC 6 interface power source. It can be connected to external 2.5V power or only connect an external capacitor 1uF when using internal LDO for 1.8V or 1.5V interface power.
FILCAP_15	B62, A71, A61	P	connect to an external capacitor 0.1uF for power supply stablization.
VDD33_SVR	A86	p	The 3.3V power for internal switching regulator
LX	B75	AO	The output of internal switching regulator and connected to an inductor 4.7uH, 1A to generate 1.1V power

Symbol	Pin	Type	Description
VDD33	A6, A10, B15, A27, A33, A36, A42	p	Analog 3.3V power input
VDD25_REG	A9	AO	The 2.5V power output
VDD25_IO	B41, B46, A63, B73	p	The 2.5V power source for IO pad
AVDDVCO_O	A12	OA	Analog 1.25V power output for VCO
AVDDVCO_I	A34	P	Analog 1.25V power input for VCO and connected to pin A12
FILCAP[0:7]	A3, B12, B18, B19, A30, B31, A39	I	Connect to an external capacitor 0.1uF for power stable.
AVDD25	A11		Analog 2.5V input. Connect this pin to pin A9 and add 0.1uF capacitor to this pin.

NOTE: For a 2-layer PCB design, we strongly recommend the use of external power — 1.1V for AVDD and DVDD. This will reduce thermal effects.

NOTE: For a four-layer PCB design, we strongly recommend the use of a reserve external power supply for AVDD and DVDD when using the internal switch regulator.

The following table shows the interface summary relative to the AR8327's different modes.

Table 1-2. **Interface Summary for MAC0, MAC6 or PHY4**

PAD name	Pin	I/O	GMII PHY mode (MAC0)	2RGMII (MAC0+ MAC6)	2RGMII (MAC0+ PHY4)
GTXCLK_0	A73	I/O	txclk_0 (O)	txclk_0 (I)	txclk_0 (I)
TXEN_0	A72	I	txen_0	txen_0	txen_0
TXD0_0	B63	I	txd0_	txd0_0	txd0_0
TXD1_0	A74	I	txd1_0	txd1_0	txd1_0
TXD2_0	B64	I	txd2_0	txd2_0	txd2_0
TXD3_0	A75	I	txd3_0	txd3_0	txd3_0
RXCLK_0	A65	O	rxclk_0 (O)	rxclk_0 (O)	rxclk_0 (O)
RXDV_0	A64	O	rxdv_0	rxdv_0	rxdv_0
RXD0_0	A68	O	rxd0_0	rxd0_0	rxd0_0
RXD1_0	A69	O	rxd1_0	rxd1_0	rxd1_0
RXD2_0	A70	O	rxd2_0	rxd2_0	rxd2_0
RXD3_0	B60	O	rxd3_0	rxd3_0	rxd3_0
GTXCLK_1	B51	I	gtxclk_0 (I)	txclk_6 (I)	txclk_phy4 (I)
TXEN_1	A58	I	—	txen_6	txctl_phy4
TXD0_1	A59	I	txd4_0	txd0_6	txd0_phy4
TXD1_1	B52	I	txd5_0	txd1_6	txd1_phy4

Table 1-2. **Interface Summary for MAC0, MAC6 or PHY4**

PAD name	Pin	I/O	GMII PHY mode (MAC0)	2RGMII (MAC0+ MAC6)	2RGMII (MAC0+ PHY4)
TXD2_1	A60	I	txd6_0	txd2_6	txd2_phy4
TXD3_1	B53	I	txd7_0	txd3_6	txd3_phy4
RXCLK_1	B47	O	—	rxclk_6 (O)	rxclk_phy4 (O)
RXDV_1	A54	O	—	rxdv_6	rxctl_phy4
RXD0_1	A55	O	rxd4_0	rxd0_6	rxd0_phy4
RXD1_1	B48	O	rxd5_0	rxd1_6	rxd1_phy4
RXD2_1	B49	O	rxd6_0	rxd2_6	rxd2_phy4
RXD3_1	A57	O	rxd7_0	rxd3_6	rxd3_phy4

2. Functional Description

The AR8327 supports many operating modes that can be configured using a low-cost serial EEPROM and/or the MDC/MDIO interface. The AR8327 also supports a CPU header mode that appends two bytes to each frame.

The CPU can deheader frame with header to configure the switch register, the address lookup table, and VLAN and receive auto-cast MIB frames. The sixth port (port5) supports a PHY interface as a WAN port. The first port (port0) supports a MAC interface and can be configured in MII-PHY or RMII-PHY mode to connect to an external management CPU or an integrated CPU in a routing or xDSL engine.

The AR8327 contains a 2 K-entry address lookup table that employs three entries per bucket to avoid hash collision and maintain non-blocking forwarding performance. The table provides read/write accesses from the serial and CPU interfaces; each entry can be configured as a static entry. The AR8327 supports 4K VLAN entries configurable as port-based VLANs or 802.1Q tag-based VLANs.

To provide non-blocking switching performance in all traffic environments, the AR8327 supports several types of QoS function with four-level priority queues based on port, IEEE 802.1p, IPv4 DSCP, IPv6 TC, 802.1Q VID, or MAC address. Back pressure and pause frame-based flow control schemes are included to support zero packet loss under temporary traffic congestion.

Meeting today's service provider requirements, the AR8327 switch uses the latest Atheros QoS switch architecture that supports ingress policing and egress rate limiting. The AR8327 device supports IPv4 IGMP snooping and IPv6 MLD snooping to significantly improve the performance of streaming media and other bandwidth-intensive IP multicast applications.

IEEE 802.3x full duplex flow control and back-pressure half duplex flow control schemes are supported to ensure zero packet loss during temporary traffic congestion.

A broadcast storm control mechanism prevents the packets from flooding into other parts of the network. The AR8327 device has an intelligent switch engine to prevent Head-of-Line blocking problems on per-CoS basis for each port.

2.1 Applications

2.1.1 AP Router Application

Figure 2-1 shows the block diagram for an AP router application. This solution is a complete end-to-end 802.AP RJ-45-to-air router 802.11n wireless network processing solution. The AR8327 eliminates the external PHY for the WAN interface. Note that the AR8327 can also work as a one-arm router.

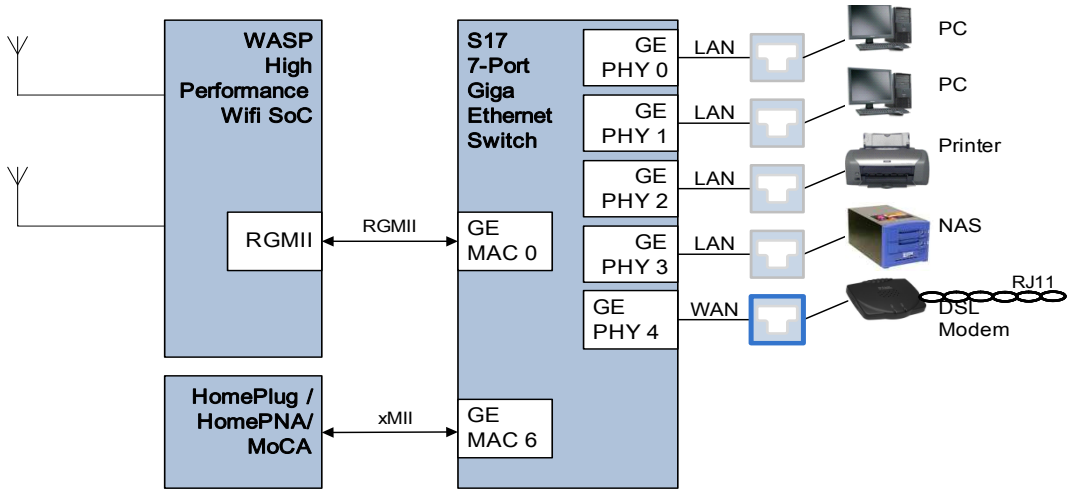


Figure 2-1. **AP Router Application**

2.2 Atheros Header

AR8327 support proprietary Atheros Header that can indicate the packet information and allow CPU to control the packet forwarding. The Header can be 2 bytes or 4 bytes with additional 2 bytes identifier. For 2 bytes header case, each packet sent out or received must include header. For 4 bytes header case, Header can exist only in the management frame and there is no header in the normal frame. The Atheros header also supports read/write register through the CPU port.

Table 2-1 shows the Type in the Atheros Header.

Table 2-1. **Atheros Header Type**

Type	Packet Type	Description
5'h0	NORMAL	NORMAL PACKET
5'h1	MIB	The packet includes MIB counter for the source port number in the header.
5'h2	Read_write_reg_ack	This packet indicates the register data for read register command or acknowledge for write register command. See read/write register in the chapter of Atheros Header receive.
5'h3	802.1x	802.1x
5'h4	Reserved MAC ADDR.	Reserved ARL
5'h5	RIPv1	RIPv1
5'h6	DHCP	DHCP
5'h7	PPPoe Discovery	PPPoE discovery
5'h8	ARP	ARP(IF ARP not found, change this type to 5'h13)
5'h9	Reserved	Reserved for RARP
5'hA	IGMP	IGMP packets
5'hB	MLD	MLD packets
5'hC	Reserved	Reserved for neighbor discovery
5'hD	Redirect to CPU	Acl_redirect_to_CPU, ARL_redirect_to_CPU offload match redirect to cpu
5'hE	normalization	The frame doesn't compliance with normal TCP/IP flow.
5'hF	LEARN LIMIT	The MAC address already reach the learning limit.
5'h10	IPv4 NAT TO CPU	1.doing NAT and TCP special status 2.doing NAT and frame is IP fragment
5'h11	IP frame: SIP not found	The SIP in IP frame doesn't pass the source check.
5'h12	NAT NOT FOUND	NAT NOT FOUND
5'h13	ARP not found	The ARP frame doesn't pass the source check.
5'h14	IP frame: routing not found	The frame DIP is not found in the routing table.
5'h15	TTL Exceed	The router try to forward one frame, but the TTL is 0 after decrease 1 and the destination is not CPU.
5'h16	MTU Exceed	The frame length exceed the MTU.
5'h17	Copy to CPU	acl_copy_to_CPU, arl_copy_to_CPU, offload match copy to cpu

Table 2-1. **Atheros Header Type**

5'h18	Mirror to CPU	Acl_mirror_to_CPU, arl_mirror_to_CPU, port_mirror_to_CPU, offload match mirror
5'h19	Flooding to CPU	Broadcast flooding to CPU, unknown unicast/multicast flooding to CPU
5'h1A	Forwarding to CPU	Bridging to CPU(ARL DP), Routing to CPU (offload match), IGMP hardware join/leave forwarding to CPU, Special DIP Header/ACL assigned DP

2.2.1 Transmit

The AR8327 will send out the frame with Atheros Header when header is enabled. The header will indicate the source port of the frame and frame type and priority. The detail format of Atheros Header is shown in Table 2-2.

Table 2-2. **Atheros Header Transmit Format Detail**

Bits	Name	Description
15:14	Version	The value is 2'b10.
13:11	priority	Frame priority.
10:6	Type	Frame Type, the next table shows the detail.
5:4	reserved	
3	Frame_with_tag	The ingress frame is Tagged.
2:0	Source_port_num	The ingress port number.

2.3 Receive

The AR8327 will recognize the Atheros Header on receive when the header is enabled. The format is depicted in Table 2-3.

Table 2-3. **Atheros Header Receive**

Bit	Name	Description
15:14	version	The version must be 2'b10
13:11	priority	
10:8		0: normal
		1: Read/write reg
		2: Disable learn
		3: Disable offload
		4: Disable Learn & offload
7	From_cpu	The bit indicates the forwarding method. 1'b1: The forwarding is based on DP_bit_map and bypass lookup. 1'b0: The forwarding is based on the lookup result.
6:0	DP_bit_map	These bits indicates the forwarding port map. See the description in the bit From_cpu.

2.4 Header for Read/Write Register.

The AR8327 supports the read/write register through the Atheros Header. The figure is the frame format of the read/write register command.

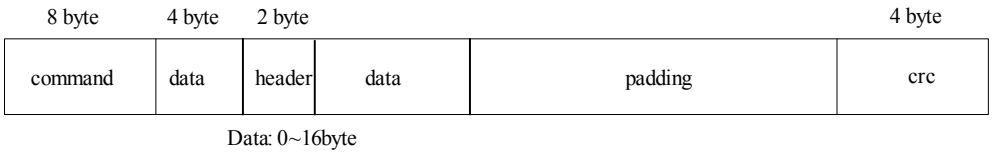


Table 2-4. **Command Format for Read/Write Register using Atheros Header**

Bit	Name	Description
18:0	ADDR	The starting register address for the read/write command. The address must be boundary of word address.
23:20	LENGTH	The data length for read/write register. Maximum 16 bytes.
28	CMD	1'b0: write 1'b1: read
31:29	CHECK_CODE	Must be 3'b101. otherwise the command would be ignored.
63:32	SEQ_NUM	The Sequence number can be checked by CPU.

2.5 Media Access Controllers (MAC)

The AR8327 integrates seven independent GB Ethernet MACs that perform all functions in the IEEE 802.3 specifications, for example, frame formatting, frame stripping, CRC checking, CSMA/CD, collision handling, and back-pressure flow control. Each MAC supports 10 Mbps, 100 Mbps, or 1000 Mbps operation in either full-duplex or half-duplex mode

2.6 Port Status Configuration

The AR8327 supports flexible port status configuration on a group or per-port basis. Each port has status registers that provide information about the port interface. The first port (port 0) MAC behaves as a PHY to allow a direct connection to an external MAC (e.g. a management CPU or a MAC inside a router). In this mode, the AR8327 drives interface clocks from a CLK pin at the desired frequency. Only full-duplex modes are supported and need to match the mode of the link partner's MAC. The second RGMII interface supports a PHY interface as a WAN port.

2.6.1 Full-Duplex Flow Control

The AR8327 device supports IEEE 802.3x full-duplex flow control, force-mode full-duplex flow control, and half-duplex backpressure.

If the link partner supports auto-negotiation, the 802.3x full-duplex flow control is auto-negotiated between the remote node and the AR8327. If the full-duplex flow control is enabled, when the free buffer space is almost empty, the AR8327 sends out an IEEE 802.3x compliant PAUSE to stop the remote device from sending more frames.

2.6.2 Half-Duplex Flow Control

Half-duplex flow control regulates the remote station to avoid dropping packets in network congestion. Back pressure is supported for half-duplex operations. When the free buffer space is almost empty, the AR8327 device transmits a jam pattern on the port and forces a collision. If the half-

duplex flow control mode is not set, the incoming packet is dropped if there is no buffer space available.

2.6.3 Inter-Packet Gap (IPG)

The IPG is the idle time between any to successive packets from the same port. The typical IPG is 9.6 µs for 10 Mbps Ethernet and 960 ns for 100 Mbps Ethernet.

2.6.4 Illegal Frames

The AR8327 discards all illegal frames such as CRC error, oversized packets (length greater than maximum length), and runt packets (length less than 64 bytes).

2.7 ACL

The AR8327 supports up to 96 ACL rule table entries. Each rule can support filtering or re-direction of the incoming packets based on the following field in the packet.

- Source MAC address
- Destination MAC address
- VID
- EtherType
- Source IP address
- Destination IP address
- Protocol
- Source TCP/UDP port number
- Destination TCP/UDP port number
- Physical Port number

When the incoming packets match an entry in the rules table, the following action can be taken defined in the result field.

- Change VID field
- Drop the packet
- change VID
- change priority

The AR8327/AR8327N can bind up to 4 rules to support 16*4 bytes keys and support up to 2 matches per packet to support different functions such as ACL+Qos, ACL+routing, etc.

2.7.1 ACL Rule

The ACL rule is constructed from a packet patters, pattern mask and action. The pattern can be defined as MAC layer or Layer 3 (IPv4 or IPv6) or user defined window.

The ACL pattern types supported by the AR8327 are listed in Table 2-5.

Table 2-5. **PatternTypes**

Value	Description
1	MAC Pattern
2	IPV4 Pattern
3	IPV6 Pattern 1
4	IPV6 Pattern 2
5	IPV6 Pattern 3
6	WINDOW Pattern

Table 2-5. **PatternTypes**

7	ENHANCED MAC Pattern
0	UNVALID Pattern

2.7.2 Action Definition

The action will be taken when the defined pattern is matched.

In the ACL rule matching, AR8327 support two match consolidation. If the key of ingress frame matched with two entries in the ACL, then these two actions will consolidate. The basic rule for consolidation is the first action will be the first priority if the related bit is active. If the related bit of the first entry is inactive, then the second entry is used. But for ACL_MATCH_INT_EN, ACL_DP_ACT and MIRROR_EN field will be the OR operation between two actions.

Table 2-6. **Action Definition**

Bits	Name	Description
80	ACL_MATCH_INT_EN	Generate interrupt
79	ACL_EG_TRNAS_BYPASS	Bypass egress QinQ result
78	ACL_RATE_EN	1'b1: use acl rate limit; 1'b0: don't use acl rate limit
77:73	ACL_RATE_SEL	Select acl rate limit (index)
72:70	ACL_DP_ACT	111:drop 011:redirect 001:copy to cpu 000:forward
69	MIRROR_EN	1'b1: mirror packet to mirror port
68	DES_PORT_OVER_EN	1'b1: use DES_PORT to determine packet Destination Port, can cross VLAN.
67:61	DES_PORT	If DES_PORT_EN set to 1'b1, these bits will be used to determine destination port.
60	ENQUEUE_PRI_OVER_EN	1'b1: use ENQUEUE_PRI to determine en-queue priority
59:57	ENQUEUE_PRI	En-queue priority
56	ARP_WCMP	1'b1: select hash
55:49	ARP_INDEX	Index of ARP table
48	ARP_INDEX_OVER_EN	Overwrite the ROUTER's Result
47:46	FORCE_L3_MODE	00: no force 01: SNAT 10: DNAT 11: RESERVED
45	LOOKUP_VID_CHANGE_EN	1'b1: lookup use VID in STAG or CTAG, determined by switch tag mode. For S-TAG mode, use STAG; for C-TAG mode, use CTAG.
44	TRANS_CTAG_CHANGE_EN	Enqueue egress translation key change en
43	TRANS_STAG_CHANGE_EN	Enqueue egress translation key change en
42	CTAG_DEI_CHANGE_EN	1'b1: frame should be send out by CTAG CFI be changed to CTAG[12]

Table 2-6. **Action Definition**

41	CTAG_PRI_REMAP_EN	1'b1: frame should be send out by CTAG priority be changed to CTAG[15:13]
40	STAG_DEI_CHANGE_EN	1'b1: frame should be send out by stag CFI be changed to STAG[12]
39	STAG_PRI_REMAP_EN	1'b1: frame should be send out by stag priority be changed to STAG[15:13]
38	DSCP_REMAP_EN	Modify the DSCP of packet. 1'b1: modify 1'b0:unmodify
37:32	DSCP	DSCP Value
31:16	CTAG	[15:13] CTAG priority [12] CFI [11:0] CTAG VID
15:0	STAG	[15:13] stag priority [12] DEI [11:0] stag VID

2.7.3 MAC Pattern

The action will be taken when the MAC Pattern is matched.

Table 2-7. **MAC Pattern**

Byte	Name	Description
3:0	DA	Destination Address
11:4	SA	Source Address
13:12	VLAN [15:13] PRIORITY [12] CFI [11:0] VID/VID Low	
		This field can be VID or VID_LOW depending upon the VID_MASK_option
15:14	TYPE	Ethertype Field
16	[7] RULE RESULT INVERSE EN	1 = Action on the rule entry is not matched. 0 = Action on the rule entry is matched.
	[6:0] SOURCE PORT	Physical source port the rule is applied to

Table 2-8. **MAC Pattern Mask**

Byte	Name	Description
5:0	DA MASK	
11:6	SA MASK	

Table 2-8. **MAC Pattern Mask**

13:12	VLAN [15:13] PRIORITY MASK	
	[12] CFI MASK	
	[11:0] VID MASK/VID HIGH	
15:14	TYPE MASK	
16	[7:6] RULE VALID	2'b00:start; 2'b01:continue; 2'b10:end; 2'b11:start&end
	[5] FRAME WITH TAG MASK	1'b1: consider FRAME_WITH_TAG 1'b0: ignore FRAME_WITH_TAG
	[4] FRAME_WITH_TAG	1'b1: tagged frame 1'b0: untagged frame
	[3] VID MASK	1'b1:mask;1'b0:range
	[2:0] RULE TYPE	These three bits must be 3'b001 to indicate the MAC rule.

2.7.4 IPv4 Pattern

The action will be taken when the IPv4 Rule is matched.

Table 2-9. **IPv4 Pattern**

Byte	Name	Description
3:0	DIP	Destination IP address
7:4	SIP	Source IP address
8	IP PROTOCOL	IP protocol
9	DSCP	DSCP field
11:10	TCP/UDP DESTINATION PORT/ TCP/UDP DESTINATION PORT LOW	TCP/UDP destination port number or low bound port number. See mask byte 14 bit 1.
13:12	TCP/UDP SOURCE PORT/ TCP/UDP SOURCE PORT LOW OR ICMP TYPE CODE	TCP/UDP source port number or low bound port number. See mask byte 14 bit 0.
14	[7] RESERVED [6] DHCPv4 [5] RIPv1	
	[4]SPORT_FIELD_TYPE	1: ICMP TYPE/CODE 0: TCP/UDP SPORT
	[3:0] RESERVED	

Table 2-9. **IPv4 Pattern**

15	[7:6] RESERVED [5:0] TCP FLAGS	
16	[7] RULE RESULT INVERSE EN [6:0] SOURCE PORT	

Table 2-10. **IPv4 Mask**

Byte	Name	Description
3:0	DIP MASK	
7:4	SIP MASK	
8	IP PROTOCOL MASK	
9	DSCP MASK	
11:10	TCP/UDP DESTINATION PORT MASK/ TCP/UDP DESTINATION PORT HIGH	This can be mask or high definition. See byte 14, bit 1.
13:12	TCP/UDP SOURCE PORT MASK/ TCP/UDP SOURCE PORT HIGH OR ICMP TYPE CODE MASK	This can be mask or high definition. See byte 14, bit 0.
14	[7] RESERVED [6] DHCPV4 MASK [5] RIPv1 MASK [4:2] RESERVED	
	[1] TCP/UDP DESTINATION MASK	Indicates the definition of bytes 11 and 10. 1'b1: mask; 1'b0: range
	[0] TCP/UDP SOURCE MASK	Indicates the definition of bytes 13 and 12. 1'b1: mask; 1'b0: range
15	[7:6] RESERVED [5:0] TCP FLAGS MASK	
16	[7:6] RULE VALID	2'b00:start; 2'b01:continue; 2'b10:end; 2'b11:start&end
	[5:3] RESERVED	
	[2:0] RULE TYPE	These three bits must be 3'b010 to indicate the IPv4 rule.

2.7.5 IPv6 Pattern

Table 2-11. **IPv6 Pattern — Pattern 1**

Byte	Name	Description
15:0	DIP	Destination IP address.
16	[7] RULE RESULT INVERSE EN	
	[6:0] SOURCE PORT	Physical source port the rule is applied to.

Table 2-12. **IPv6 Pattern — Pattern 2**

Byte	Name	Description
15:0	SIP	Source IP address.
16	[7] RULE RESULT INVERSE EN	
	[6:0] SOURCE PORT	Physical source port the rule is applied to.

Table 2-13. **IPv6 Pattern — Pattern 3**

Byte	Name	Description
0	IP PROTOCOL	
1	DSCP	
5:2	Reserved	
8:6	[19:0] IPV6 FLOW LABEL	[23:20] RESERVED
9	RESERVED	
11:10	TCP/UDP DESTINATION PORT/ TCP/UDP DESTINATION PORT LOW	The TCP/UDP destination port number or the low bound port number. See mask byte 14 bit 1 in the row of byte 11:10 and 13:12.
13:12	TCP/UDP SOURCE PORT/ TCP/UDP SOURCE PORT LOW Or ICMP TYPE CODE	The TCP/UDP source port number or the low bound port number. See mask byte 14 bit 0.

Table 2-13. **IPv6 Pattern — Pattern 3**

14	[7] RESERVED	
	[6] DHCPv6	
	[5] RESERVED	
	[4]SPORT_FIELD_TYPE	1: ICMP TYPE/CODE 0: TCP/UDP SPORT
	[3:0] RESERVED	
15	[7:6] RESERVED [5:0] TCP FLAGS	
16	[7] RULE RESULT INVERSE EN	
	[6:0] SOURCE PORT	

Table 2-14. **IPv6 Mask — Mask 1**

Byte	Name	Description
15:0	DIP Mask	
16	[7:6] RULE VALID	2'b00:start; 2'b01:continue; 2'b10:end; 2'b11:start&end
	[5:3] RESERVED	
	[2:0] RULE TYPE	These three bits must be 3'b011 to indicate the IPv6 Rule 1.

Table 2-15. **IPv6 Mask — Mask 2**

Byte	Name	Description
15:0	SIP Mask	Source IP address
16	[7:6] RULE VALID	2’b00:start, 2’b01:continue, 2’b10:end, 2’b11:start&end
	[5:3] RESERVED	
	[2:0] RULE TYPE	These three bits must be 3’b100 to indicate the IPv6 Rule 2

Table 2-16. **IPv6 Mask — Mask 3**

Byte	Name	Description
0	IP PROTOCOL	
1	DSCP	
5:2	RESERVED	
8:6	[19:0] IPV6 FLOW LABEL	[23:20] RESERVED
9	RESERVED	

Table 2-16. **IPv6 Mask — Mask 3**

11:10	TCP/UDP DESTINATION PORT/ TCP/UDP DESTINATION PORT HIGH	
13:12	TCP/UDP SOURCE PORT/ TCP/UDP SOURCE PORT HIGH Or ICMP TYPE CODE MASK	
14	[7] FORWARD TYPE MASK	
	[6] DHCPV6 MASK	
	[5] RESERVED [4:2] RESERVED	
	[1] TCP/UDP DESTINATION MASK	1'b1: mask; 1'b0: range
	[0] TCP/UDP SOURCE MASK	1'b1: mask; 1'b0: range
15	[7:6] RESERVED [5:0] TCP FLAGS MASK	
16	[7:6] RULE VALID	2'b00:start; 2'b01:continue; 2'b10:end; 2'b11:start&end
	[5:3] RESERVED	
	[2:0] RULE TYPE	These three bits must be 3'b101 to indicate the IPv6 Rule 3.

2.7.6 Window Pattern

Table 2-17. **Window Pattern**

Byte	Name	Description
15:0	DATA	
16	[7] RULE RESULT INVERSE EN	
	[6:0] SOURCE PORT	

Table 2-18. **Window Pattern Mask**

Byte	Name	Description
15:0	DATA MASK	
16	[7:6] RULE VALID	2'b00:start; 2'b01:continue; 2'b10:end; 2'b11:start&end
	[2:0] RULE TYPE	These three bits must be 3'b110 to indicate the Window Rule.

2.7.7 Enhanced MAC Pattern

Table 2-19. **Enhanced MAC Pattern**

Byte	Name	Description
5:0	DA/SA	Destination or Source address. See byte 15 bit 1
8:6	SA_LOW3/DA_LOW3	
10:9	STAG [15:13] PRIORITY [12] CFI [11:0] VID/VID LOW	
12:11	CTAG [15:13] PRIORITY [12] CFI [11:0] VID/VID LOW	
14:13	TYPE	
15	[7] FRAME WITH STAG MASK	1'b1: consider FRAME_WITH_STAG 1'b0: ignore FRAME_WITH_STAG
	[6] FRAME_WITH_STAG	1'b1: frame with STAG 1'b0: frame without STAG
	[5:2] RESERVED	
	[1] DA_SEL	1'b1: DA & SA[23:0] 1'b0: SA & DA[23:0]
	[0] SVID MASK	1'b1:mask;1'b0:range
16	[7] RULE RESULT INVERSE EN	
	[6:0] SOURCE PORT	

2.7.8 Enhanced MAC Pattern

Table 2-20. **Enhanced MAC Pattern Mask**

Byte	Name	Description
5:0	DA/SA MASK	
8:6	SA_LOW3/DA_LOW3 MASK	
10:9	STAG [15:13] PRIORITY MASK [12] CFI MASK [11:0] VID MASK /VID HIGH	
12:11	CTAG [15:13] PRIORITY MASK [12] CFI [11:0] VIDMASK /VID HIGH	

Table 2-20. **Enhanced MAC Pattern Mask**

14:13	TYPE MASK	
15	Reserved	
16	[7:6] RULE VALID	2'b00:start; 2'b01:continue; 2'b10:end; 2'b11:start&end
	[5] FRAME WITH CTAG MASK	1'b1: consider FRAME_WITH_CTAG 1'b0: ignore FRAME_WITH_CTAG
	[4] FRAME_WITH_CTAG	1'b1: frame with CTAG 1'b0: frame without CTAG
	[3] CVID MASK	1'b1:mask;1'b0:range
	[2:0] RULE TYPE	These three bits must be 3'b111 to indicate the Enhanced MAC Rule.

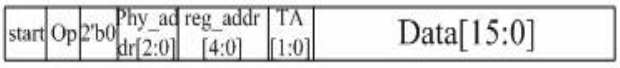
2.8 Register Access

The MDIO interface allows users to access the Switch internal registers and MII registers. The figure shown below is the format to access MII registers in the embedded PHY. The PHY address is from 0x00 up to 0x04. The Op code “10” indicates the read command and “01” is the write command.

The Switch internal registers are 32-bits wide, but the MDIO access is only 16-bits wide. So it needs 2 times access to complete the internal registers access. Moreover the address spacing is more than 10 bits supported by MDIO, So it needs to write the upper address bits to internal registers, like page mode access method. For example, the register address bit 18 to 9 are treated as page address and will be written out first as High_addr[9:0], refer the Table 1 below. Then the register could be accessed via Tables 2, where Low_addr[7:1] is the address bit [8:2] of register and Low_add[0] is 0 for Data[15:0] or Low_addr[0] is 1 for Data[31:16].

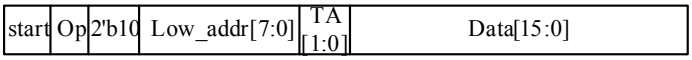
1. First, write high-address command.

Where High_Addr[9:0] is address[18:9] for register, as follows:



2. Second, read/write 32 bit register data command.

Table 2: where Low_Addr[7:1] is address [8:2] of register and Low_Addr[0] is 0 for Data[15:0], 1 for Data[31:16]



2.9 LED Control

There are totally 6 Led control rules. Three of them are used to control the LEDs of PHY 0 to PHY 3. The others are used to control the LEDs of PHY4. Each port has 3 LEDs, the default behavior of the LEDs are 1000_link_activity, 100_link_activity and 10_link_activity. The LED output is open-drain output type. So two or three of them can be connected together to indicate OR operation of the original LEDs. To achieve this operation, another way is to modify the LED control register. These LEDs also can be individually configured on or off by register.

Each LED can be controlled by 16-bits shown in the following table.

Table 2-21. **LED Control**

Bit	Name	Description
15:14	PATTERN_EN	2'b00: LED always off 2'b01: LED blinking at 4 Hz 2'b10: LED always on 2'b11: LED controlled by the following bits
13	FULL_LIGHT_EN	1'b1: LED will light when link up in full-duplex
12	HALF_LIGHT_EN	1'b1: LED will light when link up at half-duplex
11	POWER_ON_LIGHT_EN	1'b1: module should enter POWER_ON_RESET status after reset.
10	LINK_1000M_LIGHT_EN	1'b1: LED will light when link up at 1000 Mbps
9	LINK_100M_LIGHT_EN	1'b1: LED will light when link up at 100 Mbps
8	LINK_10M_LIGHT_EN	1'b1: LED will light when link up at 10 Mbps
7	COL_BLINK_EN	1'b1: LED will blink when collision is detected
6	Reserved	Must be 1'b0
5	RX_BLINK_EN	1'b1: LED will blink when receiving frame
4	TX_BLINK_EN	1'b1: LED will blink when transmitting frame
3	Reserved	Must be 1'b0
2	LINKUP_OVER_EN	1'b1: RX/TX blinking should check with LINKUP speed, LINKUP LED is ON, allow blinking. Otherwise, OFF 1'b0: RX/TX blinking will ignore the LINKUP speed.
1:0	LED_BLINK_FREQ	LED blink frequency select 2'b00: 2 HZ 2'b01: 4 Hz 2'b10: 8 Hz 2'b11: if link up at 1000Mbps, 8 Hz if link up at 100Mbps, use 4 Hz if link up at 10 Mbps, use 2 Hz

Table 2-22. **LED Rule Default Value**

Bit	Name	LED_RULE_0/1	LED_RULE_2/3	LED_RULE_4/5
	Default Value	0xCC35	0xCA35	0xC935
15:14	PATTERN_EN	2'b11	2'b11	2'b11

Table 2-22. **LED Rule Default Value (continued)**

13	FULL_LIGHT_EN	1'b0	1'b0	1'b0
12	HALF_LIGHT_EN	1'b0	1'b0	1'b0
11	POWER_ON_LIGHT_EN	1'b1	1'b1	1'b1
10	LINK_1000M_LIGHT_EN	1'b1	1'b0	1'b0
9	LINK_100M_LIGHT_EN	1'b0	1'b1	1'b0
8	LINK_10M_LIGHT_EN	1'b0	1'b0	1'b1
7	COL_BLINK_EN	1'b0	1'b0	1'b0
6	Reserved	1'b0	1'b0	1'b0
5	RX_BLINK_EN	1'b1	1'b1	1'b1
4	TX_BLINK_EN	1'b1	1'b1	1'b1
3	Reserved	1'b0	1'b0	1'b0
2	LINKUP_OVER_EN	1'b1	1'b1	1'b1
1:0	LED_BLINK_RFREQ	1'b01: 4Hz	1'b01: 4Hz	1'b01: 4Hz

2.10 VLANs

The AR8327 switch supports many VLAN options including IEEE 802.1Q and port-based VLANs. The AR8327 supports 4096 IEEE 802.1Q VLAN groups and 4K VLAN table entries, and the AR8327 device checks VLAN port membership from the VLAN ID, extracted from the tag header of the frame. Table 2-18 shows the AR8327-supported 802.1Q modes. The port-based VLAN is enabled according to the user-defined PORT VID value. The AR8327 supports optional discards of tagged, untagged frames, and priority tagged frames. The AR8327 also supports untagging of the VLAN ID for packets going out on untagged ports on a per-port basis.

The AR8327 also support double Tagging frame which is S-Tag and C-Tag. The AR8327 can lookup the 4K VLAN table by S-Tag or C-Tag depending on the configuration mode. There are also 64 entry in VLAN translation table supporting the VLAN operation.

2.10.1 Port-Based VLAN

The AR8327 switch supports port-based VLAN functionality used for non-management frames when 802.1Q is disabled on the ingress port. When FORCE_PORT_VLAN_EN is enabled, non-management frames conform to port-based configurations even if 802.1Q is enabled on the ingress port. Each ingress port contains a register that restricts the output (or egress) ports to which it can to send frames. This port-based VLAN register has a field called PORT_VID_MEM that contains the port based setting. If bit 0 of a port's PORT_VID_MEM is set to a one, the port is allowed to send frames to Port 0, bit [2] for Port 2, and so on. At reset, the PORT_VID_MEM for each port is set to a value of all 1s, except for each port's own bit, which clears to zero. Note that the CPU port is port 0.

2.10.2 802.1Q VLANs

The AR8327 supports a maximum of 4096 entries in the VLAN table. The device supports 4096 VLAN ID range from 0 to 4095. The AR8327 supports both shared and independent VLAN learning (SVL and IVL). This means that forwarding decisions are based on the frame's destination MAC address, which should be unique among all VLANs.

2.10.3 VLAN Security

The AR8327 will check the ingress packets base on the VLAN operation mode and decide forward or drop the packets. There are two sets of configuration. One is the Ingress VLAN Mode. Another is 802.1Q Mode. The Ingress VLAN Mode is checking the ingress frame is tagging or not. The 802.1Q

Mode is checking if the ingress VID is valid and if the ingress port is belong to the member. The following tables show the detail.

Table 2-23. **VLAN Security**

ING_VLAN_MODE	Frame with Tag	Frame with Priority Tagging	Frame without Tag
2'b00	Forward	Forward	Forward
2'b01	Forward	Drop	Drop
2'b10	Drop	Forward	Forward
2'b11	Forward	Forward	Forward

Table 2-24. **VLAN Security**

802.1Q	VID miss	VLAN member violation	No violation
Secure	Drop	Drop	Forward Use VLAN Table Result
Check	Drop	Forward Use VLAN Table Result	Forward Use VLAN Table Result
Fallback	Forward Use VLAN Table Result	Forward Use VLAN Table Result	Forward Use VLAN Table Result
Disable	Forward Use Port-based VLAN		

2.10.4 Port Isolation

When FORCE_PORT_VLAN_EN is enabled on the ingress port, except for VLAN member check, non-management frames will conform to port-based VLAN member check.

2.10.5 Leaky VLAN

The AR8327 support leaky VLAN to enable specific frames to be forwarded across VLAN boundary. Totally four types of frames can be leaked across VLAN boundary: Unicast, Multicast and ARP, among which Unicast and Multicast leaky are port or MAC address based and ARP is port based.

2.10.6 VLAN Translation

The AR8327 supports VLAN translation function. The AR8327 will lookup the VLAN translation table when packets arrive at the ingress port and packets transmit at the egress port.

2.10.7 VLAN Translation Table

The VLAN translation table allows user to modify the C-VID and/or S-VID. The table is shown below.

Table 2-25. **VLAN Translation Table**

Bit	Name	Description
11:0	O_VID	Original VID
23:12	S_VID	Service VID
35:24	C_VID	Custom VID

Table 2-25. **VLAN Translation Table**

37:36	ENTRY_MODE	2'b00: invalid entry 2'b01: Forward lookup enable (o -> s,c) 2'b10: Reverse lookup enable (s,c -> o) 2'b11: Forward & reverse lookup both enable.
44:38	PORT_BIT_MAP	Be used to source when frame received, destination port when frame send out.
45	O_VID_C	1'b1: use cvid 1'b0: use svid
46	S_VID_EN	1'b1: svid enable
47	C_VID_EN	1'b1: cvid enable
48	ONE_TO_ONE_MODE	1: Enanle 1:1 VLAN 0: Disable 1:1 VLAN

2.10.8 Egress Mode

The AR8327 supports per port egress VLAN mode:

- Tag mode
- Untag mode
- Unmodified
- Untouched

The frame sent out with tagged or untagged will depend on the egress mode setting. Table 2-26 shows the tagging or untagging frame on different egress mode.

Table 2-26. **VLAN Egress Mode — Tagging**

EG_VLAN_MODE	Egress VID = Untagged	Egress VID = Priority Tagged	Egress VID = Tagged
Tag	Egress Port Default VID	Egress Port Default VID	Egress VID
Unmodify	Untagged	Priority Untagged	Egress VID
Untag	Untagged	Untagged	Untagged
Untouched	Original Packet's Encapsulation		

The Egress Mode can be defined by the different operation modes, as shown in Table 2-27.

Table 2-27. **VLAN Egress Mode Definitions**

802.1Q was Disabled on Egress Port			Port-based Egress VLAN Mode
Edge Port	S-Tag Mode		Port-based Egress VLAN Mode
	C-Tag Mode		VLAN-based Egress VLAN Mode
Core Port	S-Tag Mode	S-Tag	VLAN-based Egress VLAN Mode
		C-Tag	Keep Translation Result
	C-Tag Mode	S-Tag	Keep Translation Result
		C-Tag	VLAN-based Egress VLAN Mode

2.10.9 VLAN Table

The AR8327 supports 4K VLAN membership table. It also supports the following commands to access the VLAN table:

- Read one entry
- Use get next to read out whole table
- Loading and purging of an entry
- Flush all entries, flush all of one port's entries

Table 2-28 shows the VLAN table format.

Table 2-28. **VLAN Table**

Bit	Name	Description
20	VALID	1:indicates entry is valid 0:indicates entry is empty
19	IVL_EN	1:indicates this vid is used to ivl 0:indicates this vid is used to svl, vid replaced by 0 when search mac address.
18	LEARN_LOOKUP_DIS	1:indicates no learn and not use arl table DP calculate final DP, but use uni flood DP as ARL DP to calculate DP 0:indicates normal operation about learn and final DP
17:4	EG_VLAN_MODE	5:4 for port0, 7:6 for port1 …17:16 for port6 2'b00: unmodified 2'b01: untagged 2'b10: tagged 2'b11: not member
3	PRI_ OVER_EN	Priority overwrite enable 0: keep the original VLAN priority 1: overwrite the VLAN priority with bits [2:0] of this entry
2:0	PRI	Used as frame's VLAN priority when the "PRI_OVER_EN" (bit [3]) is set to 1.

2.11 Security and Port Mapping

The AR8327 supports 802.1Q security features. Its switch discards ingress frames that do not meet security requirements and ensures those frames that do meet the requirements are sent to the designated ports only. Levels of security can be set differently on each port, and options are processed using the ingress frame’s VID:

Mode	Description
Secure	The frame is discarded if the frame’s VID is not in the VLAN table or the ingress port is not a member of the VLAN. The frame is allowed to exit only the ports that are members of the frame’s VLAN.
Check	The frame is discarded if the frame’s VID is not in the VLAN table. The frame is allowed to exit only the ports that are members of the frame’s VLAN.
Fallback	If the frame’s VID is in the VLAN table, the frame can exit only ports that are members of the frame’s VLAN. Otherwise the switch decides forwarding policy based on the port-based VLAN. If a frame arrives untagged, the AR8327 forwards based on the port-based VLAN even if the ingress port’s 802.1Q mode is enabled.
Disable	The AR8327 supports port-based egress, both unmodified and force untagged.

In these application cases, the ports work as:

Port Number	Description
Port 0	CPU Port
Port 1	LAN A
Port 2	
Port 3	LANB
Port 4	
Port 5	WAN Port

In application case 1, all LAN ports can directly send frames to each other but not to the WAN port. The CPU can send frames to all ports. A LAN port must go through the CPU port to send frames to the WAN port. Similarly, the WAN port must also go through the CPU to send frames to LAN ports,. Normally a firewall application runs in the CPU, causing traffic between the LANs and WAN to go through the host CPU. Figure 2-2 shows application case 1.

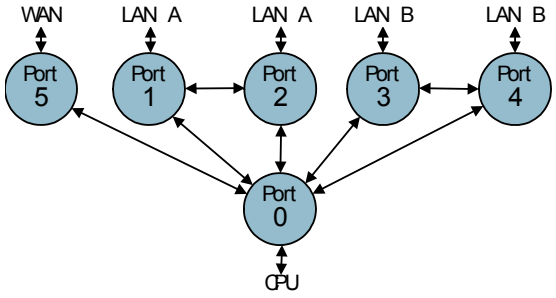


Figure 2-2. **Application Case 1**

In application case 2, the WAN port is isolated from other ports, so the switch is a five-port switch with an independent PHY. Figure 2-3 shows application case 2.

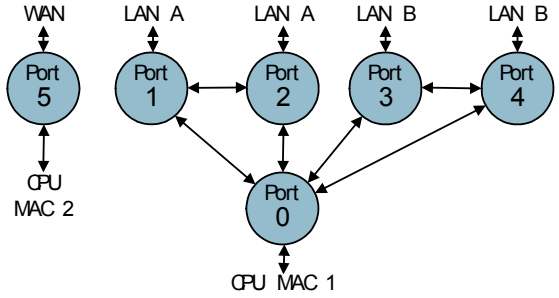


Figure 2-3. **Application Case 2**

Table 2-29. **Application Cases 1 and 2**

Member	Application Case 1		Application Case 2	
	Ports	**Description**	**Ports**	**Description**
Ports	Each port configured in 802.1Q secure mode		Each port configured in 802.1Q secure mode	
	Ports	**Create For**	**Ports**	**Create For**
VLAN1	Port 0, 1, 2	Create for LAN A	Ports 0, 1, 2	LAN A
VLAN2	Ports 0, 3, 4	Create for LAN B	Ports 0, 3, 4	LAN B
VLAN3	Ports 0, 5	Create for WAN	—	—

2.12 MIB/Statistics Counters

The statistics counter block maintains a set of forty MIB counters per port. These counters provide a set of Ethernet statistics for frames received on ingress and transmitted on egress. A register interface allows the CPU to capture, read, or clear the counter values.

The counters support:

- RMON MIB
- Ethernet-like MIB
- MIB II
- Bridge MIB
- RFC2819

The CPU interface supports:

- Autocast MIB counters after half-full
- Autocast MIB counters after time out
- Autocast MIB counters when requested
- Clearing all MIB counters

Table 2-30 describes the statistics counter for each port.

Table 2-30. **MIB Counters**

Counter	Width	Offset	Description
RxBroad	32bit	0x00	The number of good broadcast frames received
RxPause	32bit	0x04	The number of PAUSE frames received
RxMulti	32bit	0x08	The number of good multicast frames received
RxFcsErr	32bit	0x0c	The total number of frames received with a valid length, but an invalid FCS and an integral number of octets
RxAllignErr	32bit	0x10	The total number of frames received with a valid length that do not have an integral number of octets and an invalid FCS
RxUndersize	32bit	0x14	The number of frames received that are less than 64 bytes long and have a good FCS
RxFragment	32bit	0x18	The number of frames received that are less than 64 bytes long and have a bad FCS
Rx64Byte	32bit	0x1C	The number of frames received that are exactly 64 bytes long including those with errors
Rx128Byte	32bit	0x20	The number of frames received whose length is between 65 and 127 bytes, including those with errors
Rx256Byte	32bit	0x24	The number of The number of frames received whose length is between 128and 255 bytes, including those with errors
Rx512Byte	32bit	0x28	The number of frames received whose length is between 256 and 511 bytes, including those with errors

Table 2-30. **MIB Counters (continued)**

Counter	Width	Offset	Description
Rx1024Byte	32bit	0x2C	The number of frames received whose length is between 512 and 1023 bytes, including those with errors
Rx1518Byte	32bit	0x30	The number of frames received whose length is between 1024 and 1518 bytes, including those with errors
RxMaxByte	32bit	0x34	The number of frames received whose length is between 1519 and maxlength, including those with errors (Jumbo)
RxTooLong	32bit	0x38	The number of frames received whose length exceeds maxlength including those with FCS errors
RxGoodByte	64bit	0x3C:0x40	Total data octets received in a frame with a valid FCS. All frame sizes are included.
RXBadByte	64bit	0x44:0x48	Total data octets received in frame with and invalid FCS. All frame sizes are included. Pause frame is included with a valid FCS
RxOverFlow	32bit	0x4C	Total valid frames received that are discarded due to lack of buffer space
Filtered	32bit	0x50	Port disabled and unknown VID
TxBroad	32bit	0x54	Total good frames transmitted with a broadcast Destination address
TxPause	32bit	0x58	Total good PAUSE frames transmitted
TxMulti	32bit	0x5C	Total good frames transmitted with a multicast Destination address
TxUnderRun	32bit	0x60	Total valid frames discarded that were not transmitted due to transmit FIFO buffer underflow
Tx64Byte	32bit	0x64	Total frames transmitted with a length of exactly 64 bytes, including errors
Tx128Byte	32bit	0x68	Total frames transmitted with a length between 65 and 127 bytes, including those with errors
Tx256Byte	32bit	0x6C	Total frames truncated with a length between 128 and 255 bytes, including those with errors
Tx512Byte	32bit	0x70	Total frames truncated with a length between 256 and 511 bytes, including those with errors
Tx1024Byte	32bit	0x74	Total frames truncated with a length between 512 and 1023 bytes, including those with errors
Tx1518Byte	32bit	0x78	Total frames transmitted with length between 1024 and 1518, including those with errors (Jumbo)
TxMaxByte	32bit	0x7C	Total frames transmitted with length between 1519 and Maxlength, including those with errors (Jumbo)
TxOverSize	32bit	0x80	Total frames over Maxlength but transmitted truncated with bad FCS
TxByte	64bit	0x84:0x88	Total data octets transmitted from counted, including those with a bad FCS
TxCollision	32bit	0x8C	Total collisions experienced by a port during packet transmission
TxAbortCol	32bit	0x90	Total number of frames not transmitted because the frame experienced 16 transmission attempts and was discarded
TxMultiCol	32bit	0x94	Total number of successfully transmitted frames that experienced more than one collision

Table 2-30. **MIB Counters (continued)**

Counter	Width	Offset	Description
TxSingleCol	32bit	0x98	Total number of successfully transmitted frames that experienced exactly one collision
TxExcDefer	32bit	0x9C	The number of frames that deferred for an excessive period of time
TxDefer	32bit	0xA0	Total frames whose transmission was delayed on its first attempt because the medium way was busy
TXLateCol	32bit	0xA4	Total number of times a collision is detected later than 512 bit-times into the transmission of a frame

2.13 Quality of Service (QoS)

The AR8327 supports six queues (MAC0, MAC5, and MAC6) or four queues (MAC1 ~ MAC4). This egress queue schedule mechanism can be configured to one of the following modes:

Table 2-31.

Mode	Description
Strict Priority (SP)	Any packets residing in the higher priority queues transmit first. Lower priority packets transmit once these queues are emptied.
Weighted Fair Queuing	Each queue is assigned a weight that determines how many packets are sent from each priority queue.
Mix Mode	The highest one or two priority queues use SP and other queues conform to WRR

The AR8327 recognizes the QoS information of ingress frames and map to different egress priority levels. The AR8327 determines the priority of the frames based on DA, TOS/TC, VLAN, and port. Each has an enable bit that can be applied. When more than one type of priority is selected, the order in which the frame priority should be applied can be determined. Priority enable bits and select order bits are set on a by port basis at the port's base address.

Priority Determined	Description
DA	Set DA_PRI_EN bit [18] to 1'b1 and add the address to the ARL table-set priority_over_en to 1'b1. ARL priority bits [59:58] can be used as DA priority.
TOS/TC	Set IP_PRI_EN bit [16] to 1'b1, and set the IP priority mapping register (0x60–0x6C).
VLAN	Set VLAN_PRI_EN (bit [17]) to 1'b1, and set the TAG priority mapping register (0x70).

When more than one priority enable bit is set to 1'b1. (DA_PRI_SEL, IP_PRI_SEL, VLAN_PRI_SEL) can determine the order in which the frame priority should be applied. If *_PRI_SEL is set to 2'b0, frame priority is determined by that first. Otherwise, priority is determined by which *_PRI_SEL is set to 2'b01, then 2'b10, 2'b11, etc.

2.14 Mirroring

Mirroring monitors traffic for information gathering or troubleshooting higher-layer protocol operations. Users can specify that a desired mirrored-to port (sniffer port) receive a copy of all traffic passing through a designated mirrored port. The AR8327 supports mirror frames that:

- Come from an ingress specified port (ingress mirroring)
- Are destined for egress-specified port (egress mirroring)
- Mirror all ingress and egress traffic to a designated port
- Mirror frames to a specific MAC address
- ACL Mirror

2.15 Rate Limiting

In triple-play applications, the switch may need to limit the rate for all frames but continue to maintain QoS policy. The AR8327 supports ingress and egress rate limiting requirements on a per-port basis by configuring the Port Rate Limit register.

The AR8327 can also support per port per Queue based egress rate limiting. Ingress rate limit can include or exclude the consideration of Management frames and registered multicast frames, while Egress rate limit can be configured to take management frames into account.

The AR8327 can limit all frames and support rate limits from 32 Kbps to 1 Gbps at 32 Kbps granularity.

The AR8327 also supports 128 counters for ACL rule based rate limits.

2.16 Broadcast Suppression

The AR8327 supports port based broadcast suppression which can include unregistered multicast, unregistered unicast and broadcast.

2.17 IGMP/MLD Snooping

The AR8327 switch supports IPv4 IGMP snooping (v1/v2/v3 supported) and IPv6 MLD snooping. By setting the IGMP_MLD_EN bit in the FRAM_ACK_CTRL0/1 register, the AR8327 can look inside IPv4 and IPv6 packets and redirect IGMP/MLD frames to the CPU for processing.

The AR8327 also supports hardware IGMP Join and Fast Leave functions. By setting IGMP_JOIN_EN and IGMP_LEAVE_EN bits in the Port Control register, the AR8327 will update the ARL Table automatically when the AR8327 receives IGMP Join or Leave packets, and then forward it to the router port directly in the case the CPU is not acting as a router or when enabling multicast VLAN_LEAKY to bypass multicast traffic directly from the WAN to the LAN

The hardware Join/Fast Leave supports the following packets:

1. IGMPv1 Join
2. IGMPv2/MLDv1 Join/Leave
3. IGMPv3/MLDv2 report excluding NONE or including NONE

2.17.1 IEEE 802.3 Reserved Group Addresses Filtering Control

The AR8327 supports the ability to drop/redirect/copy 802.1D specified reserved group MAC addresses:

01-80-C2-00-00-04 to 01-80-C2-00-00-0F by
adding the address to ARL table.

2.17.2 802.1X

The AR8327 supports identifying EAPOL frames by their reserved group addresses. Combined with port security feature, the AR8327 can implement port based or MAC based access control.

2.17.3 Forwarding Unknown

The AR8327 can be configured to prevent the forwarding of unicast frames and multicast frames with unregistered destination MAC address on per port base. This can be done by setting UNI_FLOOD_DP and MULTI_FLOOD_DP where a bit represents a port of the AR8327.

2.17.4 MAC Limit

The AR8327 supports MAC limit on a per-port basis or a global basis. When the number of learned MAC address limit is reached, the AR8327 can be configured to forward a frame with a new source MAC address to the CPU or it can be dropped.

2.18 Spanning Tree

IEEE 802.1D Spanning Tree allows bridges to automatically prevent and resolve Layer 2 forwarding loops. Switches exchange BPDUs and configuration messages and selectively enable and disable forwarding on specified ports. A tree of active forwarding links ensures an active path between any two nodes in the networks. Spanning Tree can be enabled globally or on a per-port basis by configuring the Port Status register.

2.18.1 EEPROM Programming Format

Figure 2-4 shows the EEPROM programming format. Note that the last register should be at address 0, and the LOAD_EEPROM bit written to 1'b0 to stop the load EEPROM state machine.

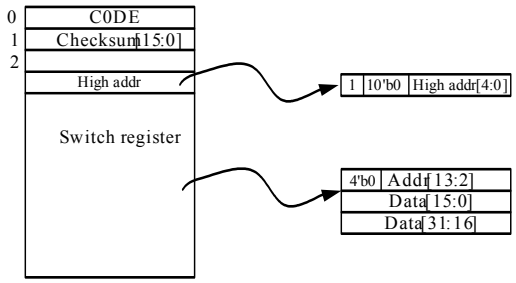


Figure 2-4. **EEPROM Programming Format**

2.18.2 Basic Switch Operation

The AR8327 automatically learns the port number of an attached end station by looking at the source MAC address of all incoming packets at wire speed. If the source address is not found in the address table, the AR8327 device adds it to the table. Once the MAC address/port number mapping is learned, all packets directed to that end station's MAC address are forwarded to the learned port number only. When the AR8327 device receives incoming packets from one of its ports, it searches in its address table for the destination MAC address, then forwards the packet to the appropriate port within the VLAN group. If the destination MAC address is not found (i.e. a new, unlearned MAC address), the AR8327 handles the packet as a broadcast packet and transmits it to all ports within the VLAN group except to the port where it came in.

2.18.3 Lookup Engine

The AR8327 lookup engine or address resolution logic (ARL) retrieves the DA and SA from each frame received from each port. The ARL performs all address searching, learning, and aging functions at wire speed. The ARL engine uses a hashing algorithm for fast storage and retrieval of address entries. To avoid hash collision, the AR8327 uses a three-entry bin per hash location that stores up to three MAC addresses at each hash location. The address database is stored in the embedded SRAM and has a size of 2048 entries.

2.18.4 Automatic Address Learning

Up to 2048 MAC address/port number mappings can be stored in the address table. A three-way hash algorithm allows a maximum of three different addresses with the same hash key to be stored simultaneously. The AR8327 searches for the SA of an incoming packet in the address table. If the SA is not found, the address is hashed and stored in the first empty bin found at the hashed location. If both address bins are full, each entry's age time is examined to select the least recently used bin. If the SA is found, the aging value of the corresponding entry is reset to 0. If the DA is PAUSE, the AR8327 automatically disables the learning process.

2.18.5 Automatic Address Aging

Address aging supports network topology changes such as an end station disconnecting from the network or an address moving from one port to another. An address is removed (aged-out) from the address database after a specified amount of time since the last time it appeared in an incoming frame source address. The AR8327 has a default aging time of 5 minutes, but can be set in 7-second increments to a maximum of 10,000 minutes.

2.18.6 Broadcast/Multicast Storm Control

If broadcast/multicast storm control is enabled, all broadcast/multicast packets beyond the default threshold of 10 ms (for 100 Mb operations) and 100 ms (for 10 Mb operations) are discarded. Atheros Header Configuration

The Atheros header is a two-byte header that the CPU uses to configure the AR8327 switch.

2.18.7 ARL Table

The address database is stored in the embedded SRAM and has a size of 2048 entries with a default aging time of about 300 seconds or 5 minutes.

Support:

- Search one address in the table
- Use get next read out whole table
- Loading and purging an entry in the ARL table
- Flush entries: all Entries, all Non-static Entries, one port's all Entries, one port's all Non-static Entries

All registers and counters can be accessed (read and written) through the UART/MDIO interface and CPU port frames. Interrupts may be asserted upon access completion.

Table 2-32.

Bit	Name	Description
83:72	VID	The VID group indicates which the MAC address belongs to
71	RESERVED	
70	COPY_TO_CPU	1'b1: A packet received with this address should be copied to the CPU port
69	REDIRECT_TO_CPU	1'b1: Indicates that a packet received with this address should be redirected to the CPU port. If no CPU is connected to the switch, this frame should be discarded.
68	LEAKY_EN	1'b1: Use Leaky VLAN enable for this MAC address. This bit can be used for Unicast and Multicast frame control by ARL_uni_leaky_en and ARL_multi_leaky_en
67:64	STATUS	4'h0: Indicates entry is empty 4'h1 ~ 7: indicates entry is dynamic and valid 4'h8 ~ 4'hE: Reserved for future use 4'F: Indicates entry is static and won't be aged out or changed by the hardware

Table 2-32.

Bit	Name	Description	
63	RESERVED		
62	SA_DROP_EN	Drop packet enable when source address is in this entry. If this bit is set to 1'b1, the packet with SA of this entry will be dropped.	
61	MIRROR_EN	1	Indicates packets should be sent to mirror port and destination port.
		0	Indicate packets should only be sent to destination port
60	PRI_EN	Priority override enable. 1: Indicates PRIORITY (ATU[58:56]) can override any other priority determined by the frame's data.	
59	SVL_ENTRY	1'b1: SVL learned 1'b0: IVL learned	
58:56	PRIORITY	The priority bits may be used as the frame's priority when "PRI_OVER_EN" (bit[60]) is set to one.	
55	CROSS_PORT_STATE_EN	1'b1: Cross port state enable 1'b0: Cross port state disable	
54:48	DES_PORT	Indicate which ports are associated with this MAC address when they are set to one. Bit [48] is assigned to port0, bit [49] to port1, bit [50] to port3, and so on. If all bits are set to zero and the entry is static, the packet should be dropped. For multicast address and unicast for link aggregation, more than one bit is set to one.	
47:0	ADDRESS	48-bit MAC address	

Table 2-33. **RESERVED ATU Entry**

Bit	Name	Description
64	STATUS	1'b1: static and valid 1'b0: invalid
63	COPY_TO_CPU	1'b1: packet received with the address should be copied to the CPU port
62	REDIRECT_TO_CPU	1'b1: packet received with this address should be redirected to the CPU port. If no CPU is connected to the switch, the packet will be dropped.
61	LEAKY_EN	1'b1: use leaky VLAN enable for this MAC address This bit can be used for unicast and multicast frames, controlled by ARL_uni_leaky_en and ARL_multi_leaky_en
60	MIRROR_EN	1'b1: indicates packets should be sent to the mirror port and the destination port 1'b0: indicates packets should be sent only to the destination port
59	PRI_OVER_EN	Priority override enable 1'b1: indicate PRIORITY (ATU[58:56]) can override any other priority determined by the frame's data
58:56	PRI	This priority bit may be used as a frame's priority when PRI_OVER_EN is set to one
55	CROSS_PORT_STATE_EN	1'b1: cross port state enabled

Table 2-33. **RESERVED ATU Entry**

Bit	Name	Description
54:48	DES_PORT	These bits indicate which ports are associated with this MAC address when they are set to '1'. Bit 48 is assigned to Port0, 49 to Port1, 50 to Port2, etc.
47:0	ADDRESS	48bit MAC address

2.19 HNAT

The AR8327N supports hardware NAT (Network Address Translation) to offload the CPU loading and achieve the full wire speed when doing the NAT. The AR8327N support the following mode of NAT.

1. Basic NAT: This involves IP address translation only, not port mapping.
2. Network Address Port Translation (NAPT): This involves the translation of both IP addresses and port numbers. For the NAPT mode, the AR8327N can support Full cone NAT, Restricted cone NAT, Port-Restricted cone NAT and Symmetric NAT.

The HNAT can automatically check the inbound and outbound traffic. If the traffic is matched the entry in the NAT or NAPT tables, then the HNAT can modify the packets accordingly without the CPU involved. For the outbound traffic from private network to public network, the HANT will do the SNAT. For the inbound traffic, the HNAT will do the DNAT.

SNAT involves the following two steps:

1. Router will use frame DIP to lookup the ARP table and use the DA in the ARP table to replace the original DA in the frame. Router will also replace the original SA with the Router MAC address.
2. NAT will replace the frame SIP and SP with the translation IP and Port number in the NAPT table.

DNAT involves the following two steps.

1. NAT will replace the frame DIP and DP with the private IP and private port number in the NAPT table.
2. Router will lookup the private IP in ARP table and will replace the DA by the MAC address in the table. Router will also replace the SA with Router MAC address.

2.19.1 Basic NAT Table

There are 32 entries in the Basic NAT table. This table is maintained by the CPU only.

Table 2-34. **Basic NAT Table**

Bit	Name	Description
79	VALID	1'b1: entry valid; 1'b0: invalid entry
78	PORT NUM EN	Port number compare enable When do SNAT, compare to frame SP When do DNAT, compare to frame DP
77:76	PROTOCOL	Protocol, compare to frame type. 2'b00:TCP 2'b01:UDP 2'b10:GRE 2'b11:Reserved
75:74	HASHKEY	The value will be compared with the hash value generated by the frame's SIP and/or SP depending on the NAT_HASH_MODE.

Table 2-34. **Basic NAT Table**

73:72	ACTION	2'b00:Mirror 2'b01:Redirect 2'b10:Copy 2'b11:forward
71	CNT EN	1'b1: counter should be add one, counter number selected by CNT INDEX
70:68	CNT INDEX	Counter index to select entry match.
67:56	PRIVATE IP	12bits private IP. The private IP is constructed under the control bit PRIVATE_IP_BASE_SEL 1'b1: these 12 bits are the private IP bit [19:16] and [7:0]. 1'b0: these 12 bits are the private IP bit [11:0]. When do SNAT, compare with frame SIP When do DNAT, used to change frame DIP
55:48	RANGE	Port number range. port number start<= port number < port number start+range
47:32	PORT NUM START	Port number start value When do SNAT, compare to frame SP. When do DNAT, compare to frame DP.
31:0	SIP	Router SIP. When do SNAT, used to change frame SIP. When do DNAT, compare with frame DIP

The lookup field will depend on the direction of the frame. For the SNAT, the SP, SIP, protocol in the frame will be used to match the corresponding field in the table. While doing DNAT, the DP, DIP, and protocol in the frame are used.

2.19.2 NAPT Entry

There are 1024 entries in the NAPT table. Each entry is 112 bits wide. The detail format is shown in Table 2-35.

Table 2-35. **NAPT Entry Table**

Bit	Name	Description
111:108	AGING FLAG	15: static 14~1: dynamic 0:entry invalid
107:104	RESERVED	
103	CNT EN	1'b1: the frame matched to this entry should be added to counter selected by CNT INDEX.
102:100	CNT INDEX	Counter index to select counter
99:98	PROTOCOL	2'b00: TCP 2'b01: UDP 2'b10: Reserved 2'b11: GRE

Table 2-35. **NAPT Entry Table**

97:96	ACTION	2'b00: Mirror 2'b01: Redirect 2'b10: Copy 2'b11: Forward
95:84	SIP	12bits private SIP. The private IP is constructed under the control bit PRIVATE_IP_BASE_SEL 1'b1: these 12 bits are the private IP bit [19:16] and [7:0]. 1'b0: these 12 bits are the private IP bit [11:0]. When do SNAT, compare with frame SIP. When do DNAT, frame DIP should be change to these bits.
83:80	TRANS IP INDEX	Translation IP index in public IP table. When do DNAT, compare with frame DIP. Use these bits to select IP address in public IP table. When do SNAT, frame SIP should be change to IP, use these bits to select IP address in public IP table.
79:64	TRANS PORT NUM	Translated Port number or Call ID When do DNAT, compare with frame DP. or CALL ID When do SNAT, frame SP should be change to these bits.
63:48	SP	When do SNAT, compare with frame SP When do DNAT, frame DP should be change to these bits
47:32	DP	When do SNAT, compare with frame DP When do DNAT, compare with frame SP
31:0	DIP	When do SNAT, compare with frame DIP When do DNAT, compare with frame SIP

2.19.3 Router MAC Address

There are 8 entries in the Router MAC address table. Each entry is 74 bits wide. The detail format is shown in Table 2-36.

Table 2-36. **Router MAC Address Table**

Bit	Name	Description
73:72	ROUTER_MAC_ACT	2'b00: invalid 2'b01: ipv4 router 2'b10: ipv6 router 2'b11: ipv4 & ipv6 router
71:60	VID_HIGH	VID range
59:48	VID_LOW	
47:0	ROUTER MAC ADDR	Router mac addressNote: DA

2.19.4 ARP ENTRY

The HNAT module supports 128 entries in the ARP table. The ARP table can be maintained by CPU. It also can be automatically learned or aged by hardware through monitoring the ARP packets. This table is used for Router function. The format of ARP table is shown below.

Table 2-37. **ARP Entry**

Bit	Name	Description
111	IP_VER	1'b1: IPv6 1'b0: IPv4
110:108	AGING_FLAG	3'h7: static 3'h1~6: valid & dynamic 3'h0: invalid
107	PPPOE EN	1'b1: add or change PPPoE header
106:103	PPPOE INDEX	PPPoE session id index, for change session or add PPPoE header.
102	CNT EN	1'b1: frame match this entry should be added to counter
101:98	CNT INDEX	Counter index to select counter.
97:96	ACTION	2'b00: Mirror 2'b01: Redirect 2'b10: Copy 2'b11: Forward
95	CPU ADDR	1'b1: this entry is for router address frame should be redirect to cpu. Normal frame, not management
94:92	SPORT NUM	When doing ARP lookup, to determine destination port number When doing source check, compare to frame SP.
91:83	VID OFFSET	Offset of VID to vid_low, vid_low+offset used to change frame VID
82:80	ROUTER MAC INDEX	Index in router mac table
79:32	MAC ADDR	When doing ARP lookup, used to change frame DA When doing source check, compare to frame SA
31:0	IP ADDR	When doing ARP lookup, compare to frame DIP When doing source check, compare to frame SIP

2.20 IEEE 802.3az and Energy Efficient Ethernet

IEEE 802.3az provides a mechanism to greatly save the power consumption between data packets burst. The link partners enter Low Power Idle state by sending short refresh signals to maintain the link.

There are two operating states, Active state for normal data transfer, and Low-power state between the data packet bursts.

In the low-power state, the AR8327 shuts off most of the analog and digital blocks to conserve energy. Due to the bursty traffic nature of Ethernet, system will stay in low-power mode in the most of time, thus the power saving can be more than 90%.

At the link start up, both link partners exchange information via auto negotiation to determine if both parties are capable of entering LPI mode.

Legacy Ethernet products are supported, and this is made transparent to the user.

2.20.1 IEEE 802.3az LPI Mode

AR8327 works in the following modes when 802.3 az feature is turned on:

- Active: the regular mode to transfer data
- Sleep: send special signal to inform remote link of entry into low-power state
- Quiet: No signal transmitted on media, most of the analog and digital blocks are turned off to reduce energy.
- Refresh: send periodically special training signal to maintain timing recovery and equalizer coefficients
- Wake: send special wake-up signal to remote link to inform of the entry back into Active.

The AR8327 supports both 100Base-Tx EEE and 1000Base-T EEE.

100Base-Tx EEE allows asymmetrical operation, which allows each link partner to enter the LPI mode independent of the other partner.

1000Base-T EEE requires symmetrical operation, which means that both link partners must enter the LPI mode simultaneously.

Figure 2-3 shows the 802.3az operating states for the AR8031.

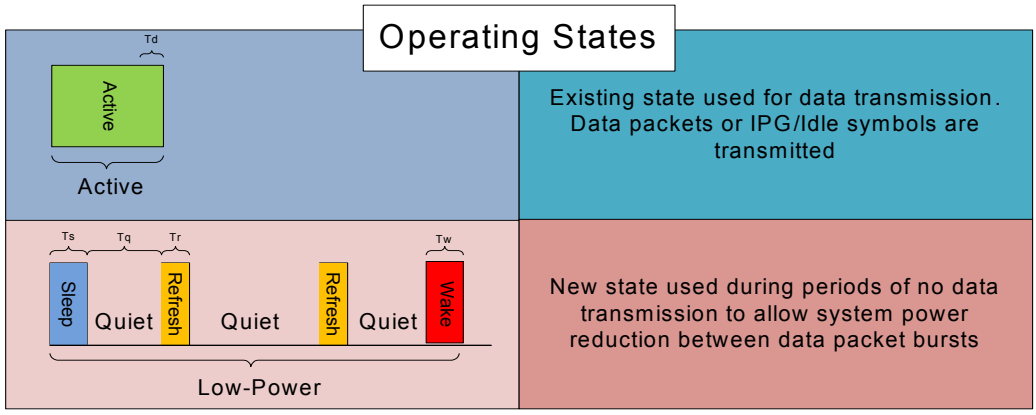


Figure 2-5. **Operating States — 802.3az LPI Mode**

Figure 2-4 shows the 802.3az operating power modes — 802.3az for the AR8327.

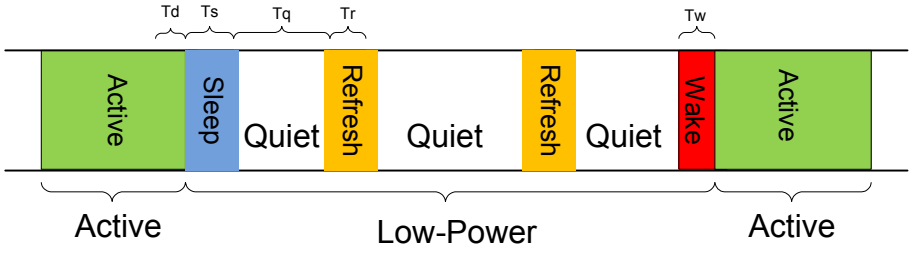


Figure 2-6. **Operating Power Modes — 802.3az LPI Mode**

Table 2-38. **Memory Map**

Register Sets	Address
Global register	0x00000 ~ 0x000FF
EEE register	0x00100 ~ 0x00AFF
Parser register	0x00200 ~ 0x003FF
ACL register	0x00400 ~ 0x005FF
Lookup register	0x00600 ~ 0x007FF
QM register	0x00800 ~ 0x00BFF
PKT Edit register	0x00C00 ~ 0x00DFF
Offload register	0x00E00 ~ 0x00FFF
Port 0 MIB counter	0x01000 ~ 0x010A7
Port 1 MIB counter	0x01100 ~ 0x011A7
Port 2 MIB counter	0x01200 ~ 0x012A7
Port 3 MIB counter	0x01300 ~ 0x013A7
Port 4 MIB counter	0x01400 ~ 0x014A7
Port 5 MIB counter	0x01500 ~ 0x015A7
Port 6 MIB counter	0x01600 ~ 0x016A7
Router MAC	0x02000 ~ 0x0207F
Public IP	0x02100 ~ 0x021FF
PPPoE session	0x02200 ~ 0x022FF
ACL Match Counter	0x1C000 ~ 0x1C0FF
Public IP	0x2A000 ~ 0x2A03F
Reserved MAC address	0x3C000 ~ 0x3C1FF
ACL Rule	0x58000 ~ 0x5FFFF
ACL Mask	0x59000 ~ 0x59FFF
ACL Action	0x5A000 ~ 0x5A7FF
Public IP	0x5AA00 ~ 0x5AAFF
Router MAC	0x5A900 ~ 0x5A97F
VLAN Translation Table	0x5AC00 ~ 0x5ADFF
PPPoE Session	0x5F000 ~ 0x5F03F

3. Register Descriptions

Table 3-1 shows the reset types used in this document.

Table 3-1. **Register Reset Types**

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.
Retain	Value written to a register field takes effect without a software reset.
RES	Reserved for future use. All reserved bits are read as zero, unless otherwise noted.
RO	Read Only.
ROC	Read Only Clear. After a read, the register field is cleared to zero.
R/W	Read/Write.
RWC	Read/Write Clear on read. All bits are readable and writable. After a reset, or after the register is read, the register field is reset to zero.
RWR	Read/Write Reset. All bits are readable and writable. After a reset, or after the register is read, the register field is cleared to zero.
RWS	Read/Write Set. All bits are readable and writable. After a reset, the register field is set to a non-zero value specified in the text.
SC	Self-Clear. Writing a one to this register causes the desired function to execute immediately, and the register field clears to zero when the function is complete.
Update	The value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.
WO	Write Only. Reads to this type of register field return undefined data.

3.1 Register Address Space (Address Range 0x0000 ~ 0x00FC)

Table 3-2 summarizes the register address space occupied by the registers.

Table 3-2. **Register Address Space Summary**

Name	Address
GLOBAL CONTROL REGISTER	0x0000~0x00FF
EEE CONTROL REGISTER	0x0100~0x01FF
PARSER CONTROL REGISTER	0x0200~0x03FF
ACL CONTROL REGISTER	0x0400~0x05FF
LOOKUP CONTROL REGISTER	0x0600~0x07FF
QM CONTROL REGISTER	0x0800~0x0BFF
PKT EDIT CONTROL REGISTER	0x0C00~0x0DFF
L3 CONTROL REGISTER	0x0E00~0x0FFF

3.2 Global Register Summary (Address Range 0x0000 ~ 0x00B4)

Table 3-3 summarizes the registers.

Table 3-3. **Register Summary**

Name	Address	Reset
MASK CONTROL REGISTER	0x0000	HARD
PAD0 MODE CONTROL REGISTER	0x0004	HARD
PAD5 MODE CONTROL REGISTER	0x0008	HARD
PAD6 MODE CONTROL REGISTER	0x000C	HARD
POWER ON STRIPT REGISTER	0x0010	HARD
GLOBAL INTERRUPT REGISTER	0x0020~0x0024	HARD & SOFT
GLOBAL INTERRUPT MASK REGISTER	0x0028~0x002C	HARD & SOFT
MODULE ENABLE CONTROL REGISTER	0x0030	HARD & SOFT
MIB FUNCTION REGISTER	0x0034	HARD & SOFT
INTERFACE HIGH ADDRESS REGISTER	0x0038	HARD & SOFT
MDIO MASTER CONTROL REGISTER	0x003C	HARD & SOFT
BIST CONTROL REGISTER	0x0040	HARD & SOFT
BIST RECOVER REGISTER	0x0044	HARD
SERVICE TAG REGISTER	0x0048	HARD & SOFT
LED CONTROL REGISTER	0x0050~0x005C	HARD
GLOBAL MAC ADDRESS	0x0060~0x0064	HARD
MAC SIZE REGISTER	0x0078	HARD & SOFT
PORT0 STATUS REGISTER	0x007C	HARD & SOFT
PORT1 STATUS REGISTER	0x0080	HARD & SOFT
PORT2 STATUS REGISTER	0x0084	HARD & SOFT
PORT3 STATUS REGISTER	0x0088	HARD & SOFT
PORT4 STATUS REGISTER	0x008C	HARD & SOFT
PORT5 STATUS REGISTER	0x0090	HARD & SOFT
PORT6 STATUS REGISTER	0x0094	HARD & SOFT
HEADER CONTROL REGISTER	0x0098	HARD & SOFT
PORT0 HEADER CONTROL REGISTER	0x009C	HARD & SOFT
PORT1 HEADER CONTROL REGISTER	0x00A0	HARD & SOFT
PORT2 HEADER CONTROL REGISTER	0x00A4	HARD & SOFT
PORT3 HEADER CONTROL REGISTER	0x00A8	HARD & SOFT
PORT4 HEADER CONTROL REGISTER	0x00AC	HARD & SOFT
PORT5 HEADER CONTROL REGISTER	0x00B0	HARD & SOFT
PORT6 HEADER CONTROL REGISTER	0x00B4	HARD & SOFT
SGMII CONTROL REGISTER	0x00E0	

3.2.1 MASK_CTRL

Address: 0x0000

HW RST

Table 3-4 summarizes the Mask Control Registers.

Table 3-4. **Master Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	W/SC	0	SOFT_RET	1'b1: software reset. This bit is set by the sofware to initate the hardware. It should be slef-cleared by the hardware after the initialization is done.
30:17	R/O	0	Reserved	
16	R/W	0	LOAD_EEPROM	load EEPROM enable. This bit is set to automatically load registers from an EEPROM. It should be cleared after the loading is complete.
15:8	RO	0x12	DEVICE_ID	Device identifier
7:0	RO	0x02	REV_ID	Revision identifier

NOTE: This register can only be reset by a hardware reset.

3.2.2 PORT0 PAD MODE CTRL HW RST

Address: 0x0004

Table 3-5 summarizes the PORT0 PAD MODE CTRL Registers

Table 3-5. **PORT0 PAD MODE CTRL Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:27	R/O	0	Reserved	
26	R/W	0	Mac0_rgmii_en	1'b1 mac0 connected to cpu through RGMII interface
25	R/W	0	Mac0_rgmii_txclk_delay_en	1'b1 RGMII interface txclk(input from cpu) will be delay, delay value depend on bit23:bit22
24	R/W	0	Mac0_rgmii_rxclk_delay_en	1'b1 RGMII interface rxclk will be delay, 1000M: delay 2ns output to cpu 10/100M: delay value depend on bit21:bit20
23:22	R/W	0	Mac0_rgmii_txclk_delay_sel	2'b11 ~ 2'b00 Control the delay value of RGMII interface txclk,2'b11 has the max delay
21:20	R/W	0	Mac0_rgmii_rxclk_delay_sel	2'b11 ~ 2'b00 Control the delay value of RGMII interface rxclk,2'b11 has the max delay

Table 3-5. **PORT0 PAD MODE CTRL Register**

Bit	R/W	Inital Value	Mnemonic	Description
19	R/W	0	SGMII_CLK125M_RX_SEL	Configure the receive clock phase for MAC interface and must be set when using SerDes or SGMII module. 0 = rising edge 1 = falling edge
18	R/W	0	SGMII_CLK125M_TX_SEL	Configure the transmit clock phase for SerDes interface 0 = rising edge 1 = falling edge
17	R/O	0	Reserved	
16	R/O	0	Reserved	
15	R/O	0	Reserved	
14	R/W	0	Mac0_phy_gmii_en	1'b1 mac0 connected to cpu through GMII interface, phy mode
13	R/W	0	Mac0_phy_gmii_txclk_sel	1'b1 select invert clock input for port0 phymode, GMII interface txclk
12	R/W	0	Mac0_phy_gmii_rxclk_sel	1'b1 select invert clock output for port0 phymode, GMII interface rxclk
11	R/W	0	Mac0_phy_mii_pipe_rxclk_sel	1'b1 select clock edge for rxpipe,default is invert
10	R/W	0	Mac0_phy_mii_en	1'b1 mac0 connected to cpu through MII interface, phy mode
9	R/W	0	Mac0_phy_mii_txclk_sel	1'b1 select invert clock output for port0 phymode ,MII interface txclk
8	R/W	0	Mac0_phy_mii_rxclk_sel	1'b1 select invert clock output for port0 phymode ,MII interface rxclk
7	R/W	0	Mac0_sgmii_en	
6	R/W	0	Mac0_mac_gmii_en	1'b1 mac0 connected to cpu through GMII interface, mac mode
5	R/W	0	Mac0_mac_gmii_txclk_sel	1'b1 select invert clock output for port0 macmode, GMII interface txclk
4	R/W	0	Mac0_mac_gmii_rxclk_sel	1'b1 select invert clock input for port0 macmode, GMII interface rxclk
3	R/O	0	RESERVED	
2	R/W	0	Mac0_mac_mii_en	1'b1 mac0 connected to cpu through MII interface, mac mode
1	R/W	0	Mac0_mac_mii_txclk_sel	1'b1 select invert clock input for port0 macmode, MII interface txclk
0	R/W	0	Mac0_mac_mii_rxclk_sel	1'b1 select invert clock input for port0 macmode, MII interface rxclk

3.2.3 PORT5 PAD MODE CTRL HW RST

Address 0x0008

Table 3-6 summarizes the PORT5 PAD MODE CTRL Register.

Table 3-6. **PORT5 PAD MODE CTRL Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:27	R/O	0	Reserved	
26	R/W	0	Mac5_rgmii_en	1'b1 Mac5 connected to cpu through RGMII interface
25	R/W	0	Mac5_rgmii_txclk_delay_en	1'b1 RGMII interface txclk(input from cpu) will be delay, delay value depend on bit23:bit22
24	R/W	0	Mac5_rgmii_rxclk_delay_en	1'b1 RGMII interface rxclk will be delay, 1000M: delay 2ns output to cpu 10/100M: delay value depend on bit21:bit20
23:22	R/W	0	Mac5_rgmii_txclk_delay_sel	2'b11 ~ 2'b00 Control the delay value of RGMII interface txclk,2'b11 has the max delay
21:20	R/W	0	Mac5_rgmii_rxclk_delay_sel	2'b11 ~ 2'b00 Control the delay value of RGMII interface rxclk,2'b11 has the max delay
19:12	R/O	0	Reserved	
11	R/W	0	Mac5_phy_mii_pipe_rxclk_sel	1'b1 select clock edge for rxpipe,default is invert
10	R/W	0	Mac5_phy_mii_en	1'b1: mac5 connected to cpu through MII interface, phy mode
9	R/W	0	Mac5_phy_mii_txclk_sel	1'b1 select invert clock output for port5 phymode ,MII interface txclk
8	R/W	0	Mac5_phy_mii_rxclk_sel	1'b1 select invert clock output for port5 phymode ,MII interface rxclk
7;3	R/W	0	Reserved	
2	R/W	0	Mac5_mac_mii_en	1'b1 Mac5 connected to cpu through MII interface, mac mode
1	R/W	0	Mac5_mac_mii_txclk_sel	1'b1 select invert clock input for port5 macmode, MII interface txclk
0	R/W	0	Mac5_mac_mii_rxclk_sel	1'b1 select invert clock input for port5 macmode, MII interface rxclk

3.2.4 PORT6 PAD MODE CTRL

Address: 0x000C

HW RST

Table 3-7 summarizes the PORT6 PAD MODE CTRL Registers.

Table 3-7. **PORT6 PAD MODE CTRL Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:27	R/O	0	Reserved	
26	R/W	0	Mac6_rgmii_en	1'b1 mac6 connected to cpu through RGMII interface
25	R/W	0	Mac6_rgmii_txclk_delay_en	1'b1 RGMII interface txclk(input from cpu) will be delay, delay value depend on bit23:bit22
24	R/W	0	Mac6_rgmii_rxclk_delay_en	1'b1 RGMII interface rxclk delay. 1000M: delay 2ns output to cpu 10/100M: delay value depend on bit21:bit20
23:22	R/W	0	Mac6_rgmii_txclk_delay_sel	2'b11 ~ 2'b00 Control the delay value of RGMII interface txclk,2'b11 has the max delay
21:20	R/W	0	Mac6_rgmii_rxclk_delay_sel	2'b11 ~ 2'b00 Control the delay value of RGMII interface rxclk,2'b11 has the max delay
19	R/O	0	RESERVED	
18	R/O	0	Phy4_mii_en	1'b1 phy4 connected to cpu through MII interface
17	R/O	0	Phy4_rgmii_en	1'b1 phy4 connected to cpu through RMII interface
16	R/O	0	Phy4_gmii_en	1'b1 phy4 connected to cpu through GMII interface
15	R/O	0	RESERVED	
14	R/W	0	Mac6_phy_gmii_en	1'b1 mac6 connected to cpu through GMII interface, phy mode
13	R/W	0	Mac6_phy_gmii_txclk_sel	1'b1 select invert clock input for port6 phymode, GMII interface txclk
12	R/W	0	Mac6_phy_gmii_rxclk_sel	1'b1 select invert clock output for port6 phymode or PHY 4, GMII interface rxclk
11	R/W	0	Mac6_phy_mii_pipe_rxclk_sel	1'b1 select clock edge for rxpipe,default is invert
10	R/W	0	Mac6_phy_mii_en	1'b1 mac6 connected to cpu through MII interface, phy mode
9	R/W	0	Mac6_phy_mii_txclk_sel	1'b1 select invert clock output for port6 phymode ,MII interface txclk
8	R/W	0	Mac6_phy_mii_rxclk_sel	1'b1 select invert clock output for port6 phymode ,MII interface rxclk
7	R/W	0	Mac6_sgmii_en	
6	R/W	0	Mac6_mac_gmii_en	1'b1 mac6 connected to cpu through GMII interface, mac mode

Table 3-7. **PORT6 PAD MODE CTRL Register**

Bit	R/W	Inital Value	Mnemonic	Description
5	R/W	0	Mac6_mac_gmii_txclk_sel	1'b1 select invert clock output for port6 macmode, GMII interface txclk
4	R/W	0	Mac6_mac_gmii_rxclk_sel	1'b1 select invert clock input for port6 macmode, GMII interface rxclk
3	R/O	0	RESERVED	
2	R/W	0	Mac6_mac_mii_en	1'b1 mac6 connected to cpu through MII interface, mac mode
1	R/W	0	Mac6_mac_mii_txclk_sel	1'b1 select invert clock input for port6 macmode, MII interface txclk
0	R/W	0	Mac6_mac_mii_rxclk_sel	1'b1 select invert clock input for port6 macmode, MII interface rxclk

3.2.5 PWS_REG

Address 0x0010

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Table 3-8 summarizes the PWS_REG Registers.

Table 3-8. **Power-on Strapping Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	POWER_ON_SEL	Power on strapping select 1 = use register configuration value to replace power on strapping for bits 25:24
30	R/W	0	PACKAGE148_EN	1 = Enable the MAC interface configuration for the 148-pin package 0 = 176-pin interface configuration
29:28	R/W	0	Reserved	
27	R/W	0	INPUT_MODE	1 = All GMII interface digital PAD work at input mode.
26	R/W	0	RESERVED	
25	R/W	0	SPI_EN_CSR	1 = EEPROM is connected to the switch
24	R/W	0	LED_OPEN_EN_CSR	1 = LED PAD is in open drain mode 0 = LED PAD is in driver mode
23:22	R/W	0	RESERVED	
21	R/W	1	RESERVED	
20:19	R/W	0	RESERVED	
18:17	R/W	1	RESERVED	
16:13	R/W	0	RESERVED	
12	R/W	1	RESERVED	
11:10	R/W	0	RESERVED	

Table 3-8. **Power-on Strapping Register**

Bit	R/W	Inital Value	Mnemonic	Description
9:8	R/W	1	RESERVED	
7	R/W	0	SERDES_AEN	SerDes auto negotiation disable 0 = enable auto negotiation 1 = disable auto negotiation
6	R/W	0	RESERVED	
5	R/W	1	RESERVED	
4:0	R/W	0	RESERVED	

3.2.6 GLOBAL_INT0

Address 0x0020

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Table 3-9 summarizes the GLOBAL_INT0 register.

Table 3-9. **Global Interrupt Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29	R/W1C	0	ACL_INI_INT	Interrupt when ACL memory initial done.
28	R/W1C	0	LOOKUP_INI_INT	Interrupt when address table initial done.(including ARL, Reserved ARL, VLAN)
27	R/W1C	0	QM_INI_INT	Interrupt when qm memory initial done.
26	R/W1C	0	MIB_INI_INT	Interrupt when mib memory initial done.
25	R/W1C	0	OFFLOAD_INI_INT	Interrupt when OFFLOAD memory initial done.
24	R/W1C	0	HARDWARE_INI_DONE	Interrupt when hardware memory initial done.
23	R/W1C	0	ACL_MATCH_INT	Interrupt when acl match(and acl_match_int_en in acl result is 1'b1)
22	R/W1C	0	ARL_DONE_INT	Interrupt when Address table was accessed done by CPU.
21	R/W1C	0	ARL_CPU_FULL_INT	Interrupt when CPU load a new address in address table, but the address's two entries are all valid.
20	R/W1C	0	VT_DONE_INT	VLAN table was accessed done by CPU.
19	R/W1C	0	MIB_DONE_INT	MIB accesse done by cpu.
18	R/W1C	0	ACL_DONE_INT	Interrupt when ACL access done by CPU
17	R/W1C	0	OFFLOAD_DONE_INT	Interrupt when OFFLOAD table access done by CPU
16	R/W1C	0	OFFLOAD_CPU_FULL_DONE_INT	Interrupt when CPU load a new entry in HNAT table, but the OFFLOAD's entries are all valid.

Table 3-9. **Global Interrupt Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
15:12	R/O	0	RESERVED	
11	R/W1C	0	ARL_LEARN_CREATE_INT	Create new entry. ARL learn a new address: Auto learn, add a new address to ARL. IGMP/MLD join a new entry: add new IGMP/MLD multicast entry to ARL
10	R/W1C	0	ARL_LEARN_CHANGE_INT	Change an existed entry. ARL learn: Auto learn, address exists. Change to new port IGMP/MLD join new port: add source port to IGMP/MLD multicast entry IGMP/MLD leave port: one port remove from the IGMP/MLD Entry
9	R/W1C	0	ARL_DELETE_INT	Delete an existing entry. AGE: age one entry from ARL(including uni/mul/igmp…) IGMP/MLD leave port: one IGMP/MLD entry is removed from ARL
8	R/W1C	0	ARL_LEARN_FULL_INT	Interrupt when learn a new address in address table, but the address's two entries are all valid.
7	R/O	0	RESERVED	
6	R/W1C	0	NAPT_AGE_DELETE_INT	NAPT AGE INTERUPT
5	R/W1C	0	ARP_LEARN_CREATE_INT	Create new entry. ARP learn a new address: Auto learn, add a new address to ARP table
4	R/W1C	0	ARP_LEARN_CHANGE_INT	Change an existed entry. ARP learn: Auto learn, address exists. Change to new port
3	R/W1C	0	ARP_AGE_DELETE_INT	Interrupt when entry removed by hardware age
2	R/W1C	0	ARP_LEARN_FULL_INT	Interrupt when learning a new address in ARP table, but table is full
1	R/W1C	0	VT_MISS_VIO_INT	Interrupt when the VID isn't in VLAN table.
0	R/W1C	0	VT_MEM_VIO_INT	Interrupt when the VID is in VLAN table, but source port isn't the member of the VID.

3.2.7 GLOBAL_INT1

Address 0x0024

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Table 3-10 summarizes the GLOBAL_INT1Register 1.

Table 3-10. **Global Interrupt Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:19	R/O	0	RESERVED	
18	R/W1C	0	EEPROM_ERR_INT	Interrupt when error occur during load eeprom.
17	R/W1C	0	EEPROM_INT	Interrupt when EEPROM load done.
16	R/W1C	0	MDIO_DONE_INT	MDIO access switch register done interrupt
15	R/W1C	0	PHY_INT	Physical layer interrupt.
14	R/W1C	0	QM_ERR_INT	Interrupt when qm detect error.
13	R/W1C	0	LOOKUP_ERR_INT	Interrupt when lookup detect error.
12	R/W1C	0	LOOP_CHECK_INT	Interrupt when loop checked by hardware
11:1	R/O	0	RESERVED	
0	R/W	0	BIST_DONE_INT	Interrupt when BIST done

3.2.8 GLOBAL_INT0

Address 0x0028

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Table 3-11 summarizes the GLOBAL_INT0 Register 0

Table 3-11. **Global Interrupt Mask Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29	R/W	0	ACL_INI_INT_EN	Enable Interrupt when ACL memory initial done
28	R/W	0	LOOKUP_INI_INT_EN	Enable Interrupt when address table initial done.(including ARL, Reserved ARL, VLAN)
27	R/W	0	QM_INI_INT_EN	Enable Interrupt when qm memory initial done
26	R/W	0	MIB_INI_INT_EN	Enable Interrupt when mib memory initial done
25	R/W	0	OFFLOAD_INI_INT_EN	Enable Interrupt when OFFLOAD memory initial done.
24	R/W	0	HARDWARE_INI_DONE_EN	Enable Interrupt when hardware memory initial done
23	R/W	0	ACL_MATCH_INT_EN	Enable Interrupt when acl match

Table 3-11. **Global Interrupt Mask Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
22			ARL_DONE_INT_EN	Enable interrupt when Address table was accessed done by CPU
21	R/W	0	ARL_CPU_FULL_INT_EN	Enable interrupt for ARL_CPU_FULL_INT
20			VT_DONE_INT_EN	Enable interrupt for VT_DONE_INT
19	R/W	0	MIB_DONE_INT_EN	Enable interrupt for MIB_DONE_INT
18	R/W	0	ACL_DONE_INT_EN	Enable interrupt for ACL_DONE_INT
17	R/W	0	OFFLOAD_DONE_INT_EN	Enable interrupt for OFFLOAD_DONE_INT
16	R/W	0	OFFLOAD_CPU_FULL_DONE_INT_EN	Enable interrupt for OFFLOAD_CPU_FULL_DONE_INT
15:12	R/W	0	RESERVED	
11	R/W	0	ARL_LEARN_CREATE_INT_EN	Enable interrupt for ARL_LEARN_CREATE_INT
10	R/W	0	ARL_LEARN_CHANGE_INT_EN	Enable interrupt for ARL_CHANGE_INT
9	R/W	0	ARL_DELETE_INT_EN	Enable interrupt for ARL_DELETE_INT
8	R/W	0	ARL_LEARN_FULL_INT_EN	Enable interrupt for ARL_LEARN_FULL_INT
7	R/W	0	RESERVED	
6	R/W	0	NAPT_AGE_DELETE_INT_EN	Enable interrupt for NAPT_AGE_DELETE_INT
5	R/W	0	ARP_LEARN_CREATE_INT_EN	Enable interrupt for ARP_LEARN_CREATE_INT
4	R/W	0	ARP_LEARN_CHANGE_INT_EN	Enable interrupt for ARP_LEARN_CHANGE_INT
3	R/W	0	ARP_AGE_DELETE_INT_EN	Enable interrupt for ARP_AGE_DELETE_INT
2	R/W	0	ARP_LEARN_FULL_INT_EN	Enable interrupt for ARP_LEARN_FULL_INT
1	R/W	0	VT_MISS_VIO_INT_EN	Enable interrupt for VT_MISS_VIO_INT
0	R/W	0	VT_MEM_VIO_INT_EN	Enable interrupt for VT_MEM_VIO_INT

3.2.9 GLOBAL_INT1

Address 0x002C

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Table 3-12 summarizes the GLOBAL_INT1 Mask Register 1.

Table 3-12. **Global Interrupt Mask Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:19	R/O	0	RESERVED	
18	R/W	0	EEPROM_ERR_INT_EN	Enable interrupt for EEPROM_ERR_INT
17	R/W	0	EEPROM_INT_EN	Enable interrupt for EEPROM_INT
16	R/W	0	MDIO_DONE_INT_EN	Enable interrupt for MDIO_DONE_INT
15	R/W	0	PHY_INT_EN	Enable interrupt for PHY_INT
14	R/W	0	QM_ERR_INT_EN	Enable interrupt for QM_ERR_INT
13	R/W	0	LOOKUP_ERR_INT_EN	Enable interrupt for LOOKUP_ERR_INT
12	R/W	0	LOOP_CHECK_INT_EN	Enable interrupt for LOOP_CHECK_INT
11:1	R/O	0	RESERVED	
0	R/W	0	BIST_DONE_INT_EN	Enable interrupt for BIST_DONE_INT

3.2.10 MODULE_EN

Address 0x0030

HW RST

Table 3-13 summarizes the MODULE_EN Register 1

Table 3-13. **Module Enable Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:10	R/O	0	RESERVED	
9	R/W	1	RESERVED	
8	R/W	1	RESERVED	
7:3	R/W	0	RESERVED	
2	R/W	0	L3_EN	1'b1: Layer 3 offload enable
1	R/W	0	ACL_EN	1'b1: acl module enable
0	R/W	0	MIB_EN	1'b1: mib count enable. If this bit set to zero, mib module won't count.

3.2.11 MIB

Address 0x0034

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Table 3-14 summarizes the MIB Function Register 1.

Table 3-14. **MIB Function Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:27	R/O	0	RESERVED	
26:24	R/W	0	MIB_FUNC	3'b000: no operation; 3'b001: flush all counters for all ports; 3'b010: reserved for future. 3'b011: capture all counters for all ports and auto-cast to cpu port; 3'b1xx:reserved for future.
23:21	R/O	0	RESERVED	
20	R/W	0	MIB_CPU_KEEP	1'b1: Does not clear MIB counter after it has been read. 1'b0: clear MIB counter to zero after read
19:18	R/O	0	RESERVED	
17	R/W SC	0	MIB_BUSY	1'b1: mib module is busy now, and can't access another new command. 1'b0: mib module is empty now, and can access new command.
16	R/W	1'b0	MIB_AT_HALF_EN	MIB auto-cast enable due to half flow. If this bit is set to 1'b1, MIB would be auto-cast when any counter's highest bit count to 1'b1.
15:0	R/W	15'h0	MIB_TIMER	MIB auto-cast timer. If these bits are set to zero, MIB won't auto-cast due to timer time out. The time is times of 8.4ms, recommended value is 'h100.

3.2.12 INTERFACE_HIGH_ADDR

Address 0x0038

HW RST

Table 3-15 summarizes the INTERFACE_HIGH_ADDR Register.

Table 3-15. **MInterface High Address Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	SPI_SPEED	1'b1: fast speed for test 1'b0: normal operation mode
30:28	R/W	0	RESERVED	
27:24	R/W	0Xf	RELOAD_TIMER	Reload EEPROM timer. If the EEPROM can't be read out, EEPROM should be reload when the timer done. It's times 8ms. If these bits are set to zero, needn't reload EEPROM.
23:20	R/W	0	RESERVED	

Table 3-15. **MInterface High Address Register**

Bit	R/W	Inital Value	Mnemonic	Description
19	R/W	0	SGMII_CLK125M_RX_SEL	SGMII interface Rx clock selection 1 = inverse clock
18	R/W	0	SGMII_CLK125M_TX_SEL	SGMII interface Tx clock selection 1 = inverse clock
17:10	R/W	0	RESERVED	
9:0	R/W	0	RESERVED	

3.2.13 MDIO Master Control

Address 0x003C

SFT&HW RST

Table 3-16 summarizes the MDIO Master Control Register

Table 3-16. **MDIO Master Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	MDIO_BUSY	1'b1: internal MDIO interface is busy. This bit should be set to 1'b1 when cpu read or write phy register through internal mdio interface, and should be clear after hardware finish the command.
30	R/O	0	MDIO_MASTER_EN	1''b1: use mdio master to config phy register. Mdc should be changed to internal mdc to phy.
29:28	R/W	0	Reserved	
27	R/O	0	MDIO_CMD	1'b0: write 1'b1: read
26	R/W	0	MDIO_SUP_PRE	1'b1: suppress preamble enable 1'b0: with 32 bits preamble
25:21	R/O	0	PHY_ADDR	Phy address
20:16	R/W	0	REG_ADDR	Phy register address
15:0	R/W	0	MDIO_DATA	When write, these bits are data written to phy register. When read, these bits are data read out from phy register.

3.2.14 BIST_CTRL

Address 0x0040

SFT&HW RST

Table 3-17 summarizes the BIST_CTRL Register.

Table 3-17. **Bist Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	BIST_BUSY	This bit should be written to 1'b1 to begin bist test and should be cleared to 1'b0 by hardware after test done. 1'b1: bist test 1'b0:bist done or idle
30	R/O		BIST_WITH_ONE_ERR	1'b1: bist test one error in data memory and can be recoverd.
29	R/O		BIST_PASS	All memory is OK, or only one error in data memory.
28:24	R/O		RESERVED	
23	R/W	0	BIST_CRITICAL	
22	R/W	0	BIST_PTN_EN_2	1'b1: enable pattern 2 for bist test
21	R/W	0	BIST_PTN_EN_1	1'b1: enable pattern 1 for bist test
20	R/W	0	BIST_PTN_EN_0	1'b1: enable pattern 0 for bist test
19:12	R/O	0	RESERVED	
11	R/O	0	OFFLOAD_BIST_DONE	
10	R/O	0	OFFLOAD_BIST_ERR	
9	R/O	0	QM_BIST_DONE	
8	R/O	0	QM_BIST_ERR	
7	R/O	0	LOOKUP_BIST_DONE	
6	R/O	0	LOOKUP_BIST_ERR	
5	R/O	0	MIB_BIST_DONE	
4	R/O	0	MIB_BIST_ERR	
3	R/O	0	ACL_BIST_DONE	
2	R/O	0	ACL_BIST_ERR	
1	R/O	0	ARB_BIST_DONE	
0	R/O	0	ARB_BIST_ERR	

3.2.15 BIST_RECOVER

Address 0x0044

HW RST

Table 3-18 summerized the BIST_RECOVER Register.

Table 3-18. **Bist Recover Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	BIST_RECOVER_EN	1'b1: enable hardware recover data memory mbist error.
30:13	R/O	0	RESERVED	
12:0	R/W	0	BIST_RECOVER_ADDR	Bist test error address of memory.

3.2.16 SERVICE_TAG

Address 0x0048

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Table 3-19 summerizes the SERVICE_TAG Register.

Table 3-19. **Service TAG Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/W	0	RESERVED	
17	R/W	0	SWITCH_STAG_MODE	Select switch work vlan mode. 1'b1: S-TAG mode 1'b0: C-TAG mode
16	R/O	0	RESERVED	
15:0	R/W	0	SERVICE_TAG	This 16-bits is used to identify the SERVICE tagged frame. When core port is enabled.

3.2.17 LED_CTRL0

Address 0x0050

HW RST

Table 3-20 summerizes LED_CTRL0 Register 0.

Table 3-20. **LED Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/W	0xCC35	LED_CTRL_RULE_1	PHY4 LED0 control rule
15:0	R/W	0xCC35	LED_CTRL_RULE_0	PHY0 ~PHY3 LED0 control rule

3.2.18 LED_CTRL1

Address 0x0054

HW RST

Table 3-21 summerizes LED_CTRL1 Register 1.

Table 3-21. **LED Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/W	0xCA35	LED_CTRL_RULE_3	PHY4 LED1 control rule
15:0	R/W	0xCA35	LED_CTRL_RULE_2	PHY0 ~PHY3 LED1 control rule

3.2.19 LED_CTRL2

Address 0x0058

HW RST

Table 3-22 Summerizes LED_CTRL2 Register 2.

Table 3-22. **LED Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/W	16'hC935	LED_CTRL_RULE_5	PHY4 LED2 control rule
15:0	R/W	16'hC935	LED_CTRL_RULE_4	PHY0 ~ PHY3 LED2 control rule

3.2.20 LED_CTRL3

Address 0x005C

HW RST

Table 3-23 summarizes the LED_CTRL3 Register 3.

Table 3-23. **LED Control Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31:26	R/W	0	RESERVED	
25:24	R/W	2'b11	LED_PATTERN_EN_32	Pattern enable for port3 LED2
23:22	R/W	2'b11	LED_PATTERN_EN_31	Pattern enable for port3 LED1
21:20	R/W	2'b11	LED_PATTERN_EN_30	Pattern enable for port3 LED0
19:18	R/W	2'b11	LED_PATTERN_EN_22	Pattern enable for port2 LED2
17:16	R/W	2'b11	LED_PATTERN_EN_21	Pattern enable for port2 LED1
15:14	R/W	2'b11	LED_PATTERN_EN_20	Pattern enable for port2 LED0
13:12	R/W	2'b11	LED_PATTERN_EN_12	Pattern enable for port1 LED2
11:10	R/W	2'b11	LED_PATTERN_EN_11	Pattern enable for port1 LED1
9:8	R/W	2'b11	LED_PATTERN_EN_10	Pattern enable for port1 LED0

Table 3-23. **LED Control Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
7:2	R/O	0	RESERVED	
1:0	R/W	2'b11	BLINK_HIGH_TIME	When led blinking, these bits determine led light time. 2'b00: 50% of blinking period. 250ms for 2Hz, 125ms for 4Hz, 62.5ms for 8Hz. 2'b01: 12.5% 2'b10: 25% 2'b11: 75%

3.2.21 GOL_MAC_ADDR0

Address 0x0060

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Table 3-24 summarizes the GOL_MAC_ADDR0 Address 0 Register.

Table 3-24. **Global MAC Address 0 Register**

Bit	R/O	Inital Value	Mnemonic	Description
31:16	R/W	0	RESERVED	
15:8	R/W	0	MAC_ADDR_BYTE4	Station address of switch, used as source address in pause frame or other management frames.
7:0	R/W	0x01	MAC_ADDR_BYTE5	

3.2.22 GOL_MAC_ADDR1

Address 0x0064

SFT&HW RST

Table 3-25 summarizes the GOL_MAC_ADDR1 Address 1 Register.

Table 3-25. **Global MAC Address 1 Register**

Bit	R/O	Inital Value	Mnemonic	Description
31:24	R/W	0	MAC_ADDR_BYTE0	
23:16	R/W	0	MAC_ADDR_BYTE1	
15:8	R/W	0	MAC_ADDR_BYTE2	
7:0	R/W	0	MAC_ADDR_BYTE3	

3.2.23 MAX_FRAME_SIZE

Address 0x0078

SFT&HW RST

Table 3-26 summarizes the MAX_FRAME_SIZE Register.

Table 3-26. **Max Frame Size Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:21	R/O	0	RESERVED	
20	R/W	0	TEST_PAUSE	Test for mac send out pause frames. Mac will send out pause on frame on posedge of this signal and pause off frame on negedge.
19	R/W	0	IPG_DEC_EN	1'b1: mac will decrease two bytes of IPG when send out frame and receive check. 1'b0: normal IPG 96 bit time
18	R/O	0	RESERVED	
17	R/O	0	RESERVED	
16	R/W	0	MAC_CRC_RESERVE_EN	1'b0`: mac will remove 4 byte crc when received frame, and add crc when transmit out frame; 1'b1`: mac won't remove 4 byte crc when received frame, and won't add crc when transmit out frame.
15:14	R/O	0	RESERVED	
13:0	R/W	'H5EE	MAX_FRAME_SIZE	Max frame size can be received and transmitted by mac. If a packet's size larger than MAX_FRAME_SIZE, it should be droped by mac. The value is for normal packet, it should be added 4 by mac if support VLAN, added 8 for double VLAN, and added 2 for Atheros header.

3.2.24 PORT0_STATUS

Address 0x007C

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Table 3-27 summarizes the PORT0_STATUS Register.

Table 3-27. **Port 0 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:13	R/O	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_0	Phy link mode enable. 1'b1: enable mac flow control config auto-neg with phy 1'b0: mac can be config by software
11	R/O	0	AUTO_RX_FLOW_EN_0	Transmit flow control enable after auto-neg.
10	R/O	0	AUTO_TX_FLOW_EN_0	Transmit flow control enable after auto-neg.
9	R/W	0	LINK_EN_0	Phy link mode enable. 1'b1: enable mac auto-neg with phy 1'b0: mac can be config by software

Table 3-27. **Port 0 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
8	R/O	0	LINK_0	Link status 1'b1: phy link up. 1'b0: phy link down.
7	R/W	0	TX_HALF_FLOW_EN_0	1'b1: transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_0	Duplex Mode. 1'b1: full-duplex mode; 1'b0: half-duplex mode.
5	R/W	0	RX_FLOW_EN_0	Rxmac Flow Control Enable.
4	R/W	0	TX_FLOW_EN_0	Txmac Flow Control Enable.
3	R/O	0	RXMAC_EN_0	Rxmac Enable.
2	R/W	0	TXMAC_EN_0	Txmac Enable.
1:0	R/W	0	SPEED_0	Speed mode. 2'b00: 10M 2'b01: 100M 2'b10: 1000M 2'b11: error speed mode

3.2.25 PORT1_STATUS

Address 0x0080

SFT&HW RST

Table 3-28 summarizes the PORT1_STATUS Register.

Table 3-28. **Port 1 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:13	R/O	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_1	Phy link mode enable. 1'b1: enable mac flow control config auto-neg with phy 1'b0: mac can be config by software
11	R/O	0	AUTO_RX_FLOW_EN_1	Transmit flow control enable after auto-neg.
10	R/O	0	AUTO_TX_FLOW_EN_1	Transmit flow control enable after auto-neg.
9	R/W	0	LINK_EN_1	Phy link mode enable. 1'b1: enable mac auto-neg with phy 1'b0: mac can be config by software
8	R/O	0	LINK_1	Link status 1'b1: phy link up. 1'b0: phy link down.
7	R/W	0	TX_HALF_FLOW_EN_1	1'b1: transmit flow control enable in half-duplex mode.

Table 3-28. **Port 1 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
6	R/W	0	DUPLEX_MODE_1	Duplex Mode. 1'b1: full-duplex mode; 1'b0: half-duplex mode.
5	R/W	0	RX_FLOW_EN_1	Rxmac Flow Control Enable.
4	R/W	0	TX_FLOW_EN_1	Txmac Flow Control Enable.
3	R/O	0	RXMAC_EN_1	Rxmac Enable.
2	R/W	0	TXMAC_EN_1	Txmac Enable.
1:0	R/W	0	SPEED_1	Speed mode. 2'b00: 10M 2'b01: 100M 2'b10: 1000M 2'b11: error speed mode

3.2.26 PORT2_STATUS

Address 0x0084

SFT&HW RST

Table 3-29 summarizes the PORT2_STATUS Register.

Table 3-29. **Port 2 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:13	R/O	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_2	Phy link mode enable. 1'b1: enable mac flow control config auto-neg with phy 1'b0: mac can be config by software
11	R/O	0	AUTO_RX_FLOW_EN_2	Transmit flow control enable after auto-neg.
10	R/O	0	AUTO_TX_FLOW_EN_2	Transmit flow control enable after auto-neg.
9	R/W	0	LINK_EN_2	Phy link mode enable. 1'b1: enable mac auto-neg with phy 1'b0: mac can be config by software
8	R/O	0	LINK_2	Link status 1'b1: phy link up. 1'b0: phy link down.
7	R/W	0	TX_HALF_FLOW_EN_2	1'b1: transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_4	Duplex Mode. 1'b1: full-duplex mode; 1'b0: half-duplex mode.
5	R/W	0	RX_FLOW_EN_2	Rxmac Flow Control Enable.
4	R/W	0	TX_FLOW_EN_2	Txmac Flow Control Enable.

Table 3-29. **Port 2 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
3	R/O	0	RXMAC_EN_2	Rxmac Enable.
2	R/W	0	TXMAC_EN_2	Txmac Enable.
1:0	R/W	0	SPEED_2	Speed mode. 2'b00: 10M 2'b01: 100M 2'b10: 1000M 2'b11: error speed mode

3.2.27 PORT3_STATUS

Address 0x0088

SFT&HW RST

Table 3-30 summarizes the PORT3_STATUS Register.

Table 3-30. **Port 3 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:13	R/O	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_3	Phy link mode enable. 1'b1: enable mac flow control config auto-neg with phy 1'b0: mac can be config by software
11	R/O	0	AUTO_RX_FLOW_EN_3	Transmit flow control enable after auto-neg.
10	R/O	0	AUTO_TX_FLOW_EN_3	Transmit flow control enable after auto-neg.
9	R/W	0	LINK_EN_3	Phy link mode enable. 1'b1: enable mac auto-neg with phy 1'b0: mac can be config by software
8	R/O	0	LINK_3	Link status 1'b1: phy link up. 1'b0: phy link down.
7	R/W	0	TX_HALF_FLOW_EN_3	1'b1: transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_3	Duplex Mode. 1'b1: full-duplex mode; 1'b0: half-duplex mode.
5	R/W	0	RX_FLOW_EN_3	Rxmac Flow Control Enable.
4	R/W	0	TX_FLOW_EN_3	Txmac Flow Control Enable.
3	R/O	0	RXMAC_EN_3	Rxmac Enable.

Table 3-30. **Port 3 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
2	R/W	0	TXMAC_EN_3	Txmac Enable.
1:0	R/W	0	SPEED_3	Speed mode. 2'b00: 10M 2'b01: 100M 2'b10: 1000M 2'b11: error speed mode

3.2.28 PORT4_STATUS

Address 0x008C

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Table 3-31 summarizes the PORT4_STATUS Register.

Table 3-31. **Port 4 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:13	R/O	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_4	Phy link mode enable. 1'b1: enable mac flow control config auto-neg with phy 1'b0: mac can be config by software
11	R/O	0	AUTO_RX_FLOW_EN_4	Transmit flow control enable after auto-neg.
10	R/O	0	AUTO_TX_FLOW_EN_4	Transmit flow control enable after auto-neg.
9	R/W	0	LINK_EN_4	Phy link mode enable. 1'b1: enable mac auto-neg with phy 1'b0: mac can be config by software
8	R/O	0	LINK_4	Link status 1'b1: phy link up. 1'b0: phy link down.
7	R/W	0	TX_HALF_FLOW_EN_4	1'b1: transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_4	Duplex Mode. 1'b1: full-duplex mode; 1'b0: half-duplex mode.
5	R/W	0	RX_FLOW_EN_4	Rxmac Flow Control Enable.
4	R/W	0	TX_FLOW_EN_4	Txmac Flow Control Enable.
3	R/O	0	RXMAC_EN_4	Rxmac Enable.

Table 3-31. **Port 4 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
2	R/W	0	TXMAC_EN_4	Txmac Enable.
1:0	R/W	0	SPEED_4	Speed mode. 2'b00: 10M 2'b01: 100M 2'b10: 1000M 2'b11: error speed mode

3.2.29 PORT5_STATUS

Address 0x0090

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Table 3-32 summarizes the PORT5_STATUS Register.

Table 3-32. **Port 5 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:13	R/O	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_5	Phy link mode enable. 1'b1: enable mac flow control config auto-neg with phy 1'b0: mac can be config by software
11	R/O	0	AUTO_RX_FLOW_EN_5	Transmit flow control enable after auto-neg.
10	R/O	0	AUTO_TX_FLOW_EN_5	Transmit flow control enable after auto-neg.
9	R/W	0	LINK_EN_5	Phy link mode enable. 1'b1: enable mac auto-neg with phy 1'b0: mac can be config by software
8	R/O	0	LINK_5	Link status 1'b1: phy link up. 1'b0: phy link down.
7	R/W	0	TX_HALF_FLOW_EN_5	1'b1: transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_5	Duplex Mode. 1'b1: full-duplex mode; 1'b0: half-duplex mode.
5	R/W	0	RX_FLOW_EN_5	Rxmac Flow Control Enable.
4	R/W	0	TX_FLOW_EN_5	Txmac Flow Control Enable.
3	R/O	0	RXMAC_EN_5	Rxmac Enable.

Table 3-32. **Port 5 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
2	R/W	0	TXMAC_EN_5	Txmac Enable.
1:0	R/W	0	SPEED_5	Speed mode. 2'b00: 10M 2'b01: 100M 2'b10: 1000M 2'b11: error speed mode

3.2.30 PORT6_STATUS

Address 0x0094

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Table 3-33 summarizes the PORT6_STATUS Register.

Table 3-33. **Port 6 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:13	R/O	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_6	Phy link mode enable. 1'b1: enable mac flow control config auto-neg with phy 1'b0: mac can be config by software
11	R/O	0	AUTO_RX_FLOW_EN_6	Transmit flow control enable after auto-neg.
10	R/O	0	AUTO_TX_FLOW_EN_6	Transmit flow control enable after auto-neg.
9	R/W	0	LINK_EN_6	Phy link mode enable. 1'b1: enable mac auto-neg with phy 1'b0: mac can be config by software
8	R/O	0	LINK_6	Link status 1'b1: phy link up. 1'b0: phy link down.
7	R/W	0	TX_HALF_FLOW_EN_6	1'b1: transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_6	Duplex Mode. 1'b1: full-duplex mode; 1'b0: half-duplex mode.
5	R/W	0	RX_FLOW_EN_6	Rxmac Flow Control Enable.
4	R/W	0	TX_FLOW_EN_6	Txmac Flow Control Enable.
3	R/O	0	RXMAC_EN_6	Rxmac Enable.

Table 3-33. **Port 6 Status Register**

Bit	R/W	Inital Value	Mnemonic	Description
2	R/W	0	TXMAC_EN_6	Txmac Enable.
1:0	R/W	0	SPEED_6	Speed mode. 2'b00: 10M 2'b01: 100M 2'b10: 1000M 2'b11: error speed mode

3.2.31 HEADER_CTRL

Address 0x0098

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Table 3-34 summarizes the HEADER_CTRL Register.

Table 3-34. **Header Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:17	R/O	0	RESERVED	
16	R/W	0	HEADER_LENGTH_SEL	0x1: 4 bytes header 0x0: 2 bytes header
15:0	R/W	0	HEADER_TYPE_VALUE	2 bytes header type added between SA & header field

3.2.32 PORT0_HEADER_CTRL

Address 0x009C

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Table 3-35 summarizes the PORT0_HEADER_CTRL Register.

Table 3-35. **PORT 0 Header Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:6	R/O	0	RESERVED	
5	R/W	0	IPG_DEC_EN_0	1'b1: mac will decrease two bytes of IPG when send out frame and receive check. 1'b0: normal IPG 96 bit time
4	R/W	0	MAC_LOOP_BACK_0	1'b1: enable mac loop back at gmii/mii interface

Table 3-35. **PORT 0 Header Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
3:2	R/W	0	RX_HEADER_MODE_0	0x0:no header; 0x1: only management with header, must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved
1:0	R/W	0	TX_HEADER_MODE_0	0x0:no header; 0x1: only management with header; must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved

3.2.33 PORT1_HEADER_CTRL

Address 0x00A0

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Table 3-36 summarizes the PORT1_HEADER_CTRL Register.

Table 3-36. **PORT 1 Header Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:6	R/O	0	RESERVED	
5	R/W	0	IPG_DEC_EN_1	1'b1: mac will decrease two bytes of IPG when send out frame and receive check. 1'b0: normal IPG 96 bit time
4	R/W	0	MAC_LOOP_BACK_1	1'b1: enable mac loop back at gmii/mii interface
3:2	R/W	0	RX_HEADER_MODE_1	0x0:no header; 0x1: only management with header, must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved
1:0	R/W	0	TX_HEADER_MODE_1	0x0:no header; 0x1: only management with header; must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved

3.2.34 PORT2_HEADER_CTRL

Address 0x00A4

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Table 3-37 summarizes the PORT2_HEADER_CTRL Register.

Table 3-37. **PORT 2 Header Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:6	R/O	0	RESERVED	
5	R/W	0	IPG_DEC_EN_2	1'b1: mac will decrease two bytes of IPG when send out frame and receive check. 1'b0: normal IPG 96 bit time
4	R/W	0	MAC_LOOP_BACK_2	1'b1: enable mac loop back at gmii/mii interface
3:2	R/W	0	RX_HEADER_MODE_2	0x0:no header; 0x1: only management with header, must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved
1:0	R/W	0	TX_HEADER_MODE_2	0x0:no header; 0x1: only management with header; must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved

3.2.35 PORT3_HEADER_CTRL

Address 0x00A8

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Table 3-38 summarizes the PORT3_HEADER_CTRL Register.

Table 3-38. **PORT 3 Header Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:6	R/O	0	RESERVED	
5	R/W	0	IPG_DEC_EN_3	1'b1: mac will decrease two bytes of IPG when send out frame and receive check. 1'b0: normal IPG 96 bit time
4	R/W	0	MAC_LOOP_BACK_3	1'b1: enable mac loop back at gmii/mii interface
3:2	R/W	0	RX_HEADER_MODE_3	0x0:no header; 0x1: only management with header, must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved
1:0	R/W	0	TX_HEADER_MODE_3	0x0:no header; 0x1: only management with header; must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved

3.2.36 PORT4_HEADER_CTRL

Address 0x00AC

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Table 3-39 summarizes the PORT4_HEADER_CTRL Register.

Table 3-39. **PORT 4 Header Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:6	R/O	0	RESERVED	
5	R/W	0	IPG_DEC_EN_4	1'b1: mac will decrease two bytes of IPG when send out frame and receive check. 1'b0: normal IPG 96 bit time
4	R/W	0	MAC_LOOP_BACK_4	1'b1: enable mac loop back at gmii/mii interface
3:2	R/W	0	RX_HEADER_MODE_4	0x0:no header; 0x1: only management with header, must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved
1:0	R/W	0	TX_HEADER_MODE_4	0x0:no header; 0x1: only management with header; must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved

3.2.37 PORT5_HEADER_CTRL

Address 0x00B0

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Table 3-40 summarizes the PORT5_HEADER_CTRL Register.

Table 3-40. **PORT 5 Header Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:6	R/O	0	RESERVED	
5	R/W	0	IPG_DEC_EN_5	1'b1: mac will decrease two bytes of IPG when send out frame and receive check. 1'b0: normal IPG 96 bit time
4	R/W	0	MAC_LOOP_BACK_5	1'b1: enable mac loop back at gmii/mii interface

Table 3-40. **PORT 5 Header Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
3:2	R/W	0	RX_HEADER_MODE_5	0x0:no header; 0x1: only management with header, must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved
1:0	R/W	0	TX_HEADER_MODE_5	0x0:no header; 0x1: only management with header; must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved

3.2.38 PORT6_HEADER_CTRL

Address 0x00B4

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Table 3-41 summarizes the PORT6_HEADER_CTRL Register.

Table 3-41. **PORT 6 Header Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:6	R/O	0	RESERVED	
5	R/W	0	IPG_DEC_EN_6	1'b1: mac will decrease two bytes of IPG when send out frame and receive check. 1'b0: normal IPG 96 bit time
4	R/W	0	MAC_LOOP_BACK_6	1'b1: enable mac loop back at gmii/mii interface
3:2	R/W	0	RX_HEADER_MODE_6	0x0:no header; 0x1: only management with header, must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved
1:0	R/W	0	TX_HEADER_MODE_6	0x0:no header; 0x1: only management with header; must be under 4 bytes header mode. 0x2: all frame with header; 0x3: reserved

3.2.39 SGMII Control Register

Address 0x00E0

SFT&HW RST

Table 3-42 summarizes the SGMII_CTRL Register.

Table 3-42. **SGMII Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	1	full_duplex_25m	Full_duplex in the base-page of base-x for Auto-Negotiation.
30	R/W	1	half_duplex_25m	half_duplex in the base-page of base-x for Auto-Negotiation.
29:28	R/W	00	Remote_fault_25m	Remote_fault[1:0] in the base-page of base-x for Auto-Negotiation. Generated by the remote_fault logic internal MAC.
27	R/W	0	Next_page_25m	Next_page index in the base-page of base-x and SGMII PHY/MAC for Auto-Negotiation.
26	R/W	1	pause_25m	pause in the base-page of base-x and SGMII-PHY/MAC for Auto-Negotiation. This part is not included in the standard for SGMII.
25	R/W	1	asym_pause_25m	asym_pause in the base-page of base-x and SGMII-PHY/MAC for Auto-Negotiation. This part is not included in the standard for SGMII.
24	R/W	1	Pause_sg_tx_en_25m	Enable transmitting pause in the base-page of base-x and SGMII-PHY/MAC for Auto-Negotiation.
23:22	R/W	0	mode_ctrl_25m	Mode_ctrl signal for mode selection among BASE-X(2'h0), SGMII-PHY(2'h1), .and SGMII-MAC(2'h2).
21	R/W	0	Mr_loopback, force_speed	Indicate loopback from MII register of cooper PHY. And Force speed control signal.
20	R/W	0	mr_reg4_ch_25m	Indicate register 4 has changed.
19	R/W	0	auto_lpi_25m	When rx_lpi_active active for once, the register will latch this to indicate that the link-partner.
18	R/W	0	Prbs_en	Enable serdes prbs test function.
17	R/W	0	Sgmii_th_los[1]	Combined with bit15, Signal detection threshold setting control 00, default; 01, -2dB; 10/11, +2dB
16	R/W	0	Dis_auto_lpi_25m	Disable the auto-detect link-partner's az ability.
15	R/W	0	Sgmii_th_los[0]	Same as bit17
14:13	R/W	11	sgmii_cdr_bw	CDR digital accumulator length control 00: +/-0, 01 : +/-2, 10: +/-4, 11: +/-8
12:10	R/W	3'b001	sgmii_txdr_ctrl	Default = 001 000, driver output Vdiff,pp=500mv 001, 600mv; 010, 700mv; 011, 800mv; 100, 900mv; 101, 1v; 110, 1.1v; 111, 1.2v
9:8	R/W	0	sgmii_fiber_mode	00, not in fiber mode 01, Reserved 10, Reserved 11, 1000Base-FX mode
7	R/W	1	sgmii_sel_clk125m	0, sgmii_clk125m_rx_delay is not delayed 1, sgmii_clk125m_rx_delay is delayed by 2ns

Table 3-42. **SGMII Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
6	R/W	1	sgmii_pll_bw	0, sgmii PLL bandwidth is low 1, sgmii PLL bandwidth is high (default)
5	R/W	0	sgmii_halftx	0, TX driver amplitude is normal (default) 1, TX driver amplitude is half
4	R/W	0	sgmii_en_sd	1, signal detection enabled 0, signal detection disabled and sgmii_fb_sdo = 0
3	R/W	1	sgmii_en_tx	1, TX driver is in idle and kept in 900mv 0, TX driver enabled
2	R/W	1	sgmii_en_rx	1, RX chain disabled, "clk125m_rx" and "dout_rx" could be any logic of 1 or 0 0, RX chain enabled
1	R/W	1	Sgmii_en_pll	1, sgmii PLL disable 0, dsgmii PLL enabled
0	R/W	0	Sgmii_en_lckdt	1, sgmii vco control voltage detector and lock detector enabled 0, disabled (default)

3.3 EEE CTRL REGISTER SUMMARY (Address Range 0x0100 ~ 0x0168)

Table 3-43 summarizes the EEE control registers.

Table 3-43. **EEE Control Register Summary**

Name	Address	Reset
EEE CONTROL REGISTER	0x0100	HARD AND SOFT
PORT1 EEE VARIABLE REGISTER	0x0120~0x0128	HARD AND SOFT
PORT2 EEE VARIABLE REGISTER	0x0130~0x0018	HARD AND SOFT
PORT3 EEE VARIABLE REGISTER	0x0140~0x0148	HARD AND SOFT
PORT4 EEE VARIABLE REGISTER	0x0150~0x0158	HARD AND SOFT
PORT5 EEE VARIABLE REGISTER	0x0160~0x0168	HARD AND SOFT

3.3.1 EEE_CTRL

Address 0x0100

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Table 3-44 summarizes the EEE_CTRL Register.

Table 3-44. **EEE Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:14	R/O	0	RESERVED	
13	R/W	0	RESERVED	
12	R/W	0	LPI_EN_5	LPI enable for PORT5
11	R/W	0	RESERVED	
10	R/W	0	LPI_EN_4	LPI enable for PORT4
9	R/W	0	RESERVED	
8	R/W	0	LPI_EN_3	LPI enable for PORT3
7	R/W	0	RESERVED	
6	R/W	0	LPI_EN_2	LPI enable for PORT2
5	R/W	0	RESERVED	
4	R/W	0	LPI_EN_1	LPI enable for PORT1, 1: disable PHY sleep 0: enable PHY sleep
3	R/W	0	EEE_CPU_CHANGE_EN	1: CPU can set the resolved value
2	R/W	0	EEE_LLDP_TO_CPU_EN	1'b1: EEE LLDP packet to CPU 1'b0: EEE LLDP packet to deheader
1	R/W	0	EEE_EN	1: support LLDP autonegation PHY wake-up time
0	R/O	0	RESERVED	

3.3.2 EEE_LOC_VALUE_1

Address 0x0120

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Table 3-45 summarizes the EEE_LOC_VALUE_1 Register 0.

Table 3-45. **PORT 1 EEE Variable Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/W	0	LOC_RX_VALUE_1	LocRxSystemValue
15:0	R/W	0	LOC_TX_VALUE_1	LocTxSystemValue

3.3.3 EEE_REM_VALUE_1

Address 0x0124

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Table 3-46 summarizes the EEE_REM_VALUE_1 Register 1.

Table 3-46. **PORT 1 EEE Variable Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/W	0	ECHO_RX_VALUE_1	LocResolvedRxSystemValueEcho
15:0	R/W	0	ECHO_TX_VALUE_1	LocResolvedTxSystemValueEcho

3.3.4 EEE_RES_VALUE_1

Address 0x0128

SFT&HW RST

Table 3-47 summarizes the EEE_RES_VALUE_1 Register 2

Table 3-47. **PORT 1 EEE Variable Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	LOC_RESOLVED_RX_VALUE_1	LocResolvedRxSystemValueEcho
15:0	R/O	0	LOC_RESOLVED _TX_VALUE_1	LocResolvedTxSystemValueEcho

3.3.5 EEE_LOC_VALUE_2

Address 0x0130

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Table 3-48 summarizes the EEE_LOC_VALUE_2 Register 0

Table 3-48. **PORT 2 EEE Variable Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/W	0	LOC_RX_VALUE_2	LocRxSystemValue
15:0	R/W	0	LOC_TX_VALUE_2	LocTxSystemValue

3.3.6 EEE_REM_VALUE_2

Address 0x0134

SFT&HW RST

Table 3-49 summarizes the EEE_REM_VALUE_2 Register 1

Table 3-49. **PORT 2 EEE Variable Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/W	0	ECHO_RX_VALUE_2	LocRxSystemValueEcho
15:0	R/W	0	ECHO_TX_VALUE_2	LocTxSystemValueEcho

3.3.7 EEE_RES_VALUE_2

Address 0x0138

SFT&HW RST

Table 3-50 summarizes the EEE_RES_VALUE_2 Register 2

Table 3-50. **PORT 2 EEE Variable Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	LOC_RESOLVED_RX_VALUE_2	LocResolvedRxSystemValueEcho
15:0	R/O	0	LOC_RESOLVED _TX_VALUE_2	LocResolvedTxSystemValueEcho

3.3.8 EEE_LOC_VALUE_3 SFT&HW RST

Address 0x0140

Table 3-51 summarizes the EEE_LOC_VALUE_3 Register 0

Table 3-51. **PORT 3 EEE Variable Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/W	0	LOC_RX_VALUE_3	LocRxSystemValue
15:0	R/W	0	LOC_TX_VALUE_3	LocTxSystemValue

3.3.9 EEE_REM_VALUE_3

Address 0x0144

SFT&HW RST

Table 3-52 summarizes the EEE_REM_VALUE_3 Register 1

Table 3-52. **PORT 3 EEE Variable Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/W	0	ECHO_RX_VALUE_3	LocRxSystemValueEcho
15:0	R/W	0	ECHO_TX_VALUE_3	LocTxSystemValueEcho

3.3.10 EEE_RES_VALUE_3

Address 0x0148

SFT&HW RST

Table 3-53 summarizes the EEE_RES_VALUE_3 Register 2

Table 3-53. **PORT 3 EEE Variable Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	LOC_RESOLVED_RX_VALUE_3	LocResolvedRxSystemValueEcho
15:0	R/O	0	LOC_RESOLVED _TX_VALUE_3	LocResolvedTxSystemValueEcho

3.3.11 EEE_LOC_VALUE_4

Address 0x0150

SFT&HW RST

Table 3-54 summarizes the EEE_LOC_VALUE_4 Register 0

Table 3-54. **PORT 4 EEE Variable Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	LOC_RX_VALUE_4	LocRxSystemValue
15:0	R/O	0	LOC_TX_VALUE_4	LocTxSystemValue

3.3.12 EEE_REM_VALUE_4

Address 0x0154

SFT&HW RST

Table 3-55 summarizes the EEE_REM_VALUE_4 Register 1

Table 3-55. **PORT 4 EEE Variable Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	ECHO_RX_VALUE_4	LocRxSystemValueEcho
15:0	R/O	0	ECHO_TX_VALUE_4	LocTxSystemValueEcho

3.3.13 EEE_RES_VALUE_4

Address 0x0158

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Table 3-56 summarizes the EEE_RES_VALUE_4 Register 2

Table 3-56. **PORT 4 EEE Variable Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	LOC_RESOLVED_RX_VALUE_4	LocResolvedRxSystemValueEcho
15:0	R/O	0	LOC_RESOLVED _TX_VALUE_4	LocResolvedTxSystemValueEcho

3.3.14 EEE_LOC_VALUE_5

Address 0x0160

SFT&HW RST

Table 3-57 summarizes the EEE_LOC_VALUE_5 Register 0

Table 3-57. **PORT 5 EEE Variable Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/W	0	LOC_RX_VALUE_5	LocRxSystemValue
15:0	R/W	0	LOC_TX_VALUE_5	LocTxSystemValue

3.3.15 EEE_REM_VALUE_5

Address 0x0164

SFT&HW RST

Table 3-58 summarizes the EEE_REM_VALUE_5 Register 1

Table 3-58. **PORT 5 EEE Variable Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/W	0	ECHO_RX_VALUE_5	LocRxSystemValueEcho
15:0	R/W	0	ECHO_TX_VALUE_5	LocTxSystemValueEcho

3.3.16 EEE_RES_VALUE_5

Address 0x0168

SFT&HW RST

Table 3-59 summarizes the Port 5 EEE Variable Register 2

Table 3-59. **PORT 5 EEE Variable Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	LOC_RESOLVED_RX_VALUE_5	LocResolvedRxSystemValueEcho
15:0	R/O	0	LOC_RESOLVED _TX_VALUE_5	LocResolvedTxSystemValueEcho

3.4 PARSER REGISTER SUMMARY(Address Range 0x0200 ~ 0x0270)

Table 3-60 summarizes the Parser registers.

Table 3-60. **Parser Register Summary**

Name	Address	Reset
NORMALIZE CONTROL REGISTER	0x0200~0x0204	HARD & SOFT
NORMALIZE LENGTH CONTROL REGISTER	0x0208	HARD & SOFT
FRAME ACK CONTROL REGISTER	0x0210~0x0214	HARD & SOFT
WINDOW RULE CONTROL REGISTER	0x0218~0x024C	HARD & SOFT
TRUNK HASH ENABLE REGISTER	0x0270	HARD & SOFT

3.4.1 NORMALIZE_CTRL0

Address 0x0200

SFT&HW RST

Table 3-61 summarizes the NORMALIZE_CTRL0 Register 0

Table 3-61. **Normalize Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29	R/W0	0	TCP_PSH1_ACK0_DROP_EN	1'b1: frame with PUSH=1 & ACK=0 should be dropped.
28	R/W0	0	TCP_FIN1_ACK0_DROP_EN	1'b1: frame with FIN=1 & ACK=0 should be dropped.
27	R/W0	0	TCP_RST1_WITH_DATA_DROP_EN	1'b1: frame with RST=1 and IP_LEN - IP_HDR_LEN - TCP_OFFSET > 0 should be dropped.
26	R/W	0	TCP_SYN1_WITH_DATA_DROP_EN	1'b1: frame with SYN=1 and IP_LEN - IP_HDR_LEN - TCP_OFFSET > 0 should be dropped.
25	R/W	0	TCP_RST1_DROP_EN	1'b1: frame with RST=1 should be dropped.
24	R/W	0	TCP_SYN0_ACK0_RST0_DROP_EN	1'b1: frame with SYN=0 & ACK=0 & RST=0 should be dropped.
23	R/W	0	TCP_SYN1_FIN1_DROP_EN	1'b1: frame with SYN=1 & FIN=ould be dropped.
22	R/W	0	TCP_SYN1_RST1_DROP_EN	1'b1: frame with SYN=1 & RST=1 should be dropped.
21	R/W	0	TCP_NULLSCAN_DROP_EN	1'b1: frame with Seq_Num=0 and all TCP FLAG zero should be dropped.

Bit	R/W	Inital Value	Mnemonic	Description
20	R/W	0	TCP_XMASSCAN_DROP_EN	1'b1: frame with Seq_Num=0, FIN=1, URG=1, and PSH=1 should be dropped
19	R/O	0	TCP_SYN1_ACK1_PSH1_DROP_EN	1'b1: frame with SYN=1 & ACK=1 & PSH=1 should be dropped.
18	R/O	0	TCP_SYN1_PSH1_DROP_EN	1'b1: frame with SYN=1 & PSH=1 should be dropped.
17	R/O	0	TCP_SYN1_URG1_DROP_EN	1'b1: frame with SYN=1 & URG=1 should be dropped.
16	R/O	0	TCP_SYN_ERR_DROP_EN	1'b1:frame with SYN=1 & ACK=0 & SP<1024,should be dropped
15	R/O	0	TCP_HDR_MIN_DROP_EN	1'b1: if frame with TCP header length less than TCP_HDR_MIN_SIZE, but not first of fragment, should be dropped
14	R/W	0	TCP_SAME_PORT_DROP_EN	1'b1: TCP frame with SP equal to DP should be dropped.
13	R/W	0	IPV4_CHECKSUM_DROP_EN	1'b1: frame with ipv4 checksum error should be dropped.
12	R/W	0	IPV4_DIP_ERR_DROP_EN	1'b1: frame should be dropped if with DIP all zero,or DIP[31:24] is 0x7F.
11	R/W	0	IPV4_SIP_ERR_DROP_EN	1'b1: frame should be dropped if with SIP[31:24] more than 0xE0 and less than 0xF0, or equal to 0x7F, or SIP[31:0] is 0x32'hFFFFFFFF.
10	R/W	0	IPV4_FRAG_LEN_DROP_EN	1'b1: frame with ipv4 fragment length check error should be dropped.
9	R/W	0	IPV4_FRAG_MAX_DROP_EN	
8	R/W	0	IPV4_FRAG_MIN_DROP_EN	1'b1: frame with offset length less than min should be dropped
7	R/W	0	IPV4_DF_DROP_EN	1'b1: frame with DF=1 and offset or MF not zero, should be dropped
6	R/W	0	IP_LEN_DROP_EN	1'b1: frame with ip length field error should be drop? include ipv4 and ipv6
5	R/W	0	IPV4_HDR_LEN_CHECK_EN	1'b1 :Check the IP options. If Frame is with options, drop or send to cpu
4	R/W	0	IPV4_HDR_LEN_ DROP_EN	This bit can be used to forward or drop frame when ipv4 header length check fail.
3	R/O	0	IPV4_HDR_LEN_MIN_DROP_EN	1'b0:frame with ipv4 header length check error should be sent to cpu port(only to cpu port)
2	R/W	0	IP_SAME_PORT_DROP_EN	1'b1: frame with ipv4 header length check error should be drop

Bit	R/W	Inital Value	Mnemonic	Description
1	R/W	0	IP_VER_DROP_EN	1'b1: frame should be dropped if ipv4 header length less than 20 byte
0	R/W	0	VID_4095_DROP_EN	1'b1: frame should be drop if sip equal to dip.

3.4.2 NORMALIZE_CTRL1

Address 0x0204

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Table 3-62 summarizes the NORMALIZE_CTRL1 Register 1

Table 3-62. **Normalize Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/W	0	IPV4_FRAG_MIN	
23:21	R/0	0	RESERVED	
20	R/W	0	INVALID_MAC_SRC_ADDR_DROP_EN	SA is broadcast or multicast address. The frame will be dropped by the switch.
19	R/W	0	IPV4_MIN_PKT_LEN_DROP_EN	If the frame length is less than the min IPv4 frame size.
18	R/W	0	IPV6_MIN_PKT_LEN_DROP_EN	If the frame length is less than the min IPv6 frame size
17	R/W	0	INVALID_SIP6_DROP_EN	Drop Invalid Source IP for IPv6 IP is ::1 or ff00::/8
16	R/W	0	INVALID_DIP6_DROP_EN	Drop Invalid Destination IP for IPv6 \ IP is ::1 or ::/128
15:12	R/W	0	TCP_HDR_MIN_SIZE	Defined the min size of TCP header
11	R/W	0	ICMP_CHECKSUM_DROP_EN	Drop the ICMP checksum error
10	R/W	0	ICMPV6_FRAG_DROP_EN	1'b1: frame with fragment ICMPV6 should be dropped.
9	R/W	0	ICMPV4_FRAG_DROP_EN	1'b1: frame with fragment ICMPV4 should be dropped.
8	R/W	0	ICMPV6_MAX_LEN_DROP_EN	1'b1: frame with un-fragment ICMPV6 length larger than ICMPV6_MAX_LEN should be dropped.
7	R/W	0	ICMPV4_MAX_LEN_DROP_EN	1'b1: frame with un-fragment ICMPV4 length larger than ICMPV4_MAX_LEN should be dropped.
6	R/W	0	UDP_CHECKSUM_DROP_EN	1'b1: frame with UDP checksum error should be dropped.

Bit	R/W	Inital Value	Mnemonic	Description
5	R/W	0	UDP_LEN_DROP_EN	1'b1: frame with UDP length check error should be dropped.
4	R/W	0	UDP_SAME_PORT_DROP_EN	1'b1: UDP frame with SP equal to DP should be dr opped.
3	R/W	0	TCP_OPTION_DROP_EN	1'b1: frame with SYN=0 and IP header larger than 20 byte, should be dropped.
2	R/W	0	TCP_URG0_PTR_ERR_DROP_EN	1'b1: frame with URG=0 but pointer not zeor should be dropped.
1	R/W	0	TCP_CHECKSUM_DROP_EN	1'b1: frame with TCP checksum error should be dropped.
0	R/W	0	TCP_URG1_ACK0_DROP_EN	1'b1: frame with URG=1 & ACK=0 should be dropped.

3.4.3 NORMALIZE_LEN_CTRL

Address 0x0208

SFT&HW RST

Table 3-63 summarizes the NORMALIZE_LEN_CTRL Register

Table 3-63. **Normalize Length Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29:16	R/W	0x40	ICMPV6_MAX_LEN	Defined the max IP payload lenght of ICMPv6 frame
15:14	R/O	0	RESERVED	
13:0	R/W	0x40	ICMPV4_MAX_LEN	Defined the max IP payload lenght of ICMPv4 frame

3.4.4 FRAM_ACK_CTRL0

Address 0x00210

SFT&HW RST

Table 3-64 summarizes the FRAM_ACK_CTRL0 Register 0

Table 3-64. **Frame Ack Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30	R/W	1'b0	ARP_REQ_EN_3	See bit 6
29	R/W	1'b0	ARP_ACK_EN_3	See bit 5
28	R/W	0	DHCP_EN_3	See bit 4
27	R/W	0	EAPOL_EN_3	See bit 3
26	R/W	0	IGMP_LEAVE_EN_3	See bit 2
25	R/W	0	IGMP_JOIN_EN_3	See bit 1
24	R/W	0	IGMP_MLD_EN_3	See bit 0
23	R/O	0	RESERVED	
22	R/W	1'b0	ARP_REQ_EN_2	See bit 6
21	R/W	1'b0	ARP_ACK_EN_2	See bit 5
20	R/W	0	DHCP_EN_2	See bit 4
19	R/W	0	EAPOL_EN_2	See bit 3
18	R/W	0	IGMP_LEAVE_EN_2	See bit 2
17	R/W	0	IGMP_JOIN_EN_2	See bit 1
16	R/W	0	IGMP_MLD_EN_2	See bit 0
15	R/W	0	RESERVED	
14	R/W	0	ARP_REQ_EN_1	See bit 6
13	R/W	0	ARP_ACK_EN_1	See bit 5
12	R/W	0	DHCP_EN_1	See bit 4
11	R/W	0	EAPOL_EN_1	See bit 3
10	R/W	0	IGMP_LEAVE_EN_1	See bit 2
9	R/W	0	IGMP_JOIN_EN_1	See bit 1
8	R/W	0	IGMP_MLD_EN_1	See bit 0
7	R/O	0	RESERVED	
6	R/W	1'b0	ARP_REQ_EN_0	ARP request frame acknowledge enable.
5	R/W	1'b0	ARP_ACK_EN_0	ARP response frame acknowledge enable
4	R/W	0	DHCP_EN_0	1'b1: acknowledge DHCP frame enable 1'b0: don't acknowledge DHCP frame
3	R/W	0	EAPOL_EN_0	1'b1: hardware acknowledge 802.1x frame, and send frame copy or redirect to cpu controlled by "EAPAL_REDIRECT_EN"
2	R/W	0	IGMP_LEAVE_EN_0	1'b1: enable IGMP/MLD hardware fast leave.

Bit	R/W	Inital Value	Mnemonic	Description
1	R/W	0	IGMP_JOIN_EN_0	1'b1: enable IGMP/MLD hardware join.
0	R/W	0	IGMP_MLD_EN_0	IGMP/MLD snooping enable. If this bit is set to 1'b1, the port will examine all received frames and copy or redirect to cpu port controlled by IGMP_COPY_EN.

3.4.5 FRAM_ACK_CTRL1

Address 0x00214

SFT&HW RST

Table 3-65 summarizes the FRAM_ACK_CTRL1 Register 1

Table 3-65. **Frame Ack Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:26	R/O	0	RESERVED	
25	R/W	0	PPPOE_EN	
24	R/W	0	IGMP_V3_EN	
23	R/W	0	RESERVED	
22			ARP_REQ_EN_6	See bit 6
21	R/W	0	ARP_ACK_EN_6	See bit 5
20			DHCP_EN_6	See bit 4
19	R/O	0	EAPOL_EN_6	See bit 3
18	R/O	0	IGMP_LEAVE_EN_6	See bit 2
17	R/O	0	IGMP_JOIN_EN_6	See bit 1
16	R/O	0	IGMP_MLD_EN_6	See bit 0
15	R/O	0	RESERVED	
14			ARP_REQ_EN_5	See bit 6
13			ARP_ACK_EN_5	See bit 5
12			DHCP_EN_5	See bit 4
11	R/W	0	EAPOL_EN_5	See bit 3
10	R/W	0	IGMP_LEAVE_EN_5	See bit 2
9	R/W	0	IGMP_JOIN_EN_5	See bit 1
8	R/W	0	IGMP_MLD_EN_5	See bit 0
7	R/W	0	RESERVED	
6	R/W	0	ARP_REQ_EN_4	ARP request frame acknowledge enable.
5	R/W	0	ARP_ACK_EN_4	ARP response frame acknowledge enable

Bit	R/W	Inital Value	Mnemonic	Description
4	R/W	0	DHCP_EN_4	1'b1: acknowledge DHCP frame enable 1'b0: don't acknowledge DHCP frame
3	R/O	0	EAPOL_EN_4	1'b1: hardware acknowledge 802.1x frame, and send frame copy or redirect to cpu controlled by "EAPAL_REDIRECT_EN"
2	R/W	0	IGMP_LEAVE_EN_4	1'b1: enable IGMP/MLD hardware fast leave.
1	R/W	0	IGMP_JOIN_EN_4	1'b1: enable IGMP/MLD hardware join.
0	R/W	0	IGMP_MLD_EN_4	IGMP/MLD snooping enable. If this bit is set to 1'b1, the port will examine all received frames and copy or redirect to cpu port controlled by IGMP_COPY_EN.

3.4.6 WIN_RULE_CTRL0

Address 0x0218

SFT&HW RST

Table 3-66 summarizes the WIN_RULE_CTRL0 Register 0

Table 3-66. **Window Rule Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27:24	R/W	0	L4_LENGTH_0	These bit indicate that window rule in port0 to select length of L4, from L4_OFFSET_0.
23:20	R/W	0	L3_LENGTH_0	These bit indicate that window rule in port0 to select length of L3, from L3_OFFSET_0.
19:16	R/W	0	L2_LENGTH_0	These bit indicate that window rule in port0 to select length of L2, from L2_OFFSET_0.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_0	These bit indicate that window rule in port0 to select offset of L3, from TCP/UDP header.
9:5	R/W	0	L3_OFFSET_0	These bit indicate that window rule in port0 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_0	These bit indicate that window rule in port0 to select offset of L2, from MAC DA.

3.4.7 WIN_RULE_CTRL1

Address 0x021C

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Table 3-67 summarizes the WIN_RULE_CTRL1 Register 1

Table 3-67. **Window Rule Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27:24	R/W	0	L4_LENGTH_1	These bit indicate that window rule in port0 to select length of L4, from L4_OFFSET_1.
23:20	R/W	0	L3_LENGTH_1	These bit indicate that window rule in port0 to select length of L3, from L3_OFFSET_1.
19:16	R/W	0	L2_LENGTH_1	These bit indicate that window rule in port0 to select length of L2, from L2_OFFSET_1.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_1	These bit indicate that window rule in port0 to select offset of L3, from TCP/UDP header.
9:5	R/W	0	L3_OFFSET_1	These bit indicate that window rule in port0 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_1	These bit indicate that window rule in port0 to select offset of L2, from MAC DA.

3.4.8 WIN_RULE_CTRL2

Address 0x0220

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Table 3-68 summarizes the WIN_RULE_CTRL2 Register 2

Table 3-68. **Window Rule Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27:24	R/W	0	L4_LENGTH_2	These bit indicate that window rule in port0 to select length of L4, from L4_OFFSET_2.
23:20	R/W	0	L3_LENGTH_2	These bit indicate that window rule in port0 to select length of L3, from L3_OFFSET_2.
19:16	R/W	0	L2_LENGTH_2	These bit indicate that window rule in port0 to select length of L2, from L2_OFFSET_2.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_2	These bit indicate that window rule in port0 to select offset of L3, from TCP/UDP header.
9:5	R/W	0	L3_OFFSET_2	These bit indicate that window rule in port0 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_2	These bit indicate that window rule in port0 to select offset of L2, from MAC DA.

3.4.9 WIN_RULE_CTRL3

Address 0x0224

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Table 3-69 summarizes WIN_RULE_CTRL3 Register 3

Table 3-69. **Window Rule Control Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27:24	R/W	0	L4_LENGTH_3	These bit indicate that window rule in port0 to select length of L4, from L4_OFFSET_3.
23:20	R/W	0	L3_LENGTH_3	These bit indicate that window rule in port0 to select length of L3, from L3_OFFSET_3.
19:16	R/W	0	L2_LENGTH_3	These bit indicate that window rule in port0 to select length of L2, from L2_OFFSET_3.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_3	These bit indicate that window rule in port0 to select offset of L3, from TCP/UDP header.
9:5	R/W	0	L3_OFFSET_3	These bit indicate that window rule in port0 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_3	These bit indicate that window rule in port0 to select offset of L2, from MAC DA.

3.4.10 WIN_RULE_CTRL4

Address 0x0228

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Table 3-70 summarizes WIN_RULE_CTRL4 Register 4

Table 3-70. **Window Rule Control Register 4**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27:24	R/W	0	L4_LENGTH_4	These bit indicate that window rule in port0 to select length of L4, from L4_OFFSET_4.
23:20	R/W	0	L3_LENGTH_4	These bit indicate that window rule in port0 to select length of L3, from L3_OFFSET_4.
19:16	R/W	0	L2_LENGTH_4	These bit indicate that window rule in port0 to select length of L2, from L2_OFFSET_4.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_4	These bit indicate that window rule in port0 to select offset of L3, from TCP/UDP header.

Bit	R/W	Inital Value	Mnemonic	Description
9:5	R/W	0	L3_OFFSET_4	These bit indicate that window rule in port0 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_4	These bit indicate that window rule in port0 to select offset of L2, from MAC DA.

3.4.11 WIN_RULE_CTRL5

Address 0x022C

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Table 3-71 summarizes the WIN_RULE_CTRL5 Register 5

Table 3-71. **Window Rule Control Register 5**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27:24	R/W	0	L4_LENGTH_5	These bit indicate that window rule in port0 to select length of L4, from L4_OFFSET_5.
23:20	R/W	0	L3_LENGTH_5	These bit indicate that window rule in port0 to select length of L3, from L3_OFFSET_5.
19:16	R/W	0	L2_LENGTH_5	These bit indicate that window rule in port0 to select length of L2, from L2_OFFSET_5.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_5	These bit indicate that window rule in port0 to select offset of L3, from TCP/ UDP header.
9:5	R/W	0	L3_OFFSET_5	These bit indicate that window rule in port0 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_5	These bit indicate that window rule in port0 to select offset of L2, from MAC DA.

3.4.12 WIN_RULE_CTRL6

Address 0x0230

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Table 3-72 summarizes the WIN_RULE_CTRL6 Register 6

Table 3-72. **Window Rule Control Register 6**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27:24	R/W	0	L4_LENGTH_6	These bit indicate that window rule in port0 to select length of L4, from L4_OFFSET_6.
23:20	R/W	0	L3_LENGTH_6	These bit indicate that window rule in port0 to select length of L3, from L3_OFFSET_6.
19:16	R/W	0	L2_LENGTH_6	These bit indicate that window rule in port0 to select length of L2, from L2_OFFSET_6.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_6	These bit indicate that window rule in port0 to select offset of L3, from TCP/UDP header.
9:5	R/W	0	L3_OFFSET_6	These bit indicate that window rule in port0 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_6	These bit indicate that window rule in port0 to select offset of L2, from MAC DA.

3.4.13 WIN_RULE_CTRL7

Address 0x0234

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Table 3-73 summarizes the WIN_RULE_CTRL7 Register 7

Table 3-73. **Window Rule Control Register 7**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_0	These bit indicate that window rule in port0 to select length of L3, from L3_OFFSET1_0.
19:16	R/W	0	L2_LENGTH1_0	These bit indicate that window rule in port0 to select length of L2, from L2_OFFSET1_0.
15:10	R/W	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_0	These bit indicate that window rule in port0 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET1_0	These bit indicate that window rule in port0 to select offset of L2, from the end of snap

3.4.14 WIN_RULE_CTRL8

Address 0x0238

SFT&HW RST

Table 3-74 summarizes the WIN_RULE_CTRL8 Register 8

Table 3-74. **Window Rule Control Register 8**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_1	
19:16	R/W	0	L2_LENGTH1_1	
15:10	R/O	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_1	
4:0	R/W	0	L2_OFFSET1_1	

3.4.15 WIN_RULE_CTRL9

Address 0x023C

SFT&HW RST

Table 3-75 summarizes the WIN_RULE_CTRL9 Register 9

Table 3-75. **Window Rule Control Register 9**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_2	
19:16	R/W	0	L2_LENGTH1_2	
15:10	R/O	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_2	
4:0	R/W	0	L2_OFFSET1_2	

3.4.16 WIN_RULE_CTRL10

Address 0x0240

SFT&HW RST

Table 3-76 summarizes the WIN_RULE_CTRL10 Register 10

Table 3-76. **Window Rule Control Register 10**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_3	
19:16	R/W	0	L2_LENGTH1_3	
15:10	R/W	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_3	
4:0	R/W	0	L2_OFFSET1_3	

3.4.17 WIN_RULE_CTRL11

Address 0x0244

SFT&HW RST

Table 3-77 summarizes the WIN_RULE_CTRL11 Register 11

Table 3-77. **Window Rule Control Register 11**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_4	
19:16	R/W	0	L2_LENGTH1_4	
15:10	R/W	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_4	
4:0	R/W	0	L2_OFFSET1_4	

3.4.18 WIN_RULE_CTRL12

Address 0x0248

SFT&HW RST

Table 3-78 summarizes the WIN_RULE_CTRL11 Register 12

Table 3-78. **Window Rule Control Register 12**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_5	

Bit	R/W	Inital Value	Mnemonic	Description
19:16	R/W	0	L2_LENGTH1_5	
15:10	R/W	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_5	
4:0	R/W	0	L2_OFFSET1_5	

3.4.19 WIN_RULE_CTRL13

Address 0x024C

SFT&HW RST

Table 3-79 summarizes the WIN_RULE_CTRL13 Register 13

Table 3-79. **Window Rule Control Register 13**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_6	
19:16	R/W	0	L2_LENGTH1_6	
15:10	R/W	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_6	
4:0	R/W	0	L2_OFFSET1_6	

3.4.20 TRUNK_HASH_EN

Address 0x0270

SFT&HW RST

Table 3-80 summarizes the TRUNK_HASH_EN Register

Table 3-80. **Trunk Hash Enable Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:4	R/O	0	RESERVED	
3	R/W	0	TRUNK_HASH_SIP_EN	SIP join the trunk hash
2	R/W	0	TRUNK_HASH_DIP_EN	DIP join the trunk hash
1	R/W	0	TRUNK_HASH_SA_EN	SA join the trunk hash
0	R/W	0	TRUNK_HASH_DA_EN	DA join the trunk hash

3.5 ACL REGISTER (Address Range: 0x0400 ~ 0x0454)

Table 3-81 summarizes the ACL registers.

Table 3-81. **ACL Register Summary**

Name	Address	Reset
ACL FUNCTION REGISTER	0x0400~0x0414	HARD & SOFT
PRIVATE CONTROL REGISTER	0x0418	HARD & SOFT
PORT0 VLAN CONTROL REGISTER	0x0420~0x0424	HARD & SOFT
PORT1 VLAN CONTROL REGISTER	0x0428~0x042C	HARD & SOFT
PORT2 VLAN CONTROL REGISTER	0x0430~0x0434	HARD & SOFT
PORT3 VLAN CONTROL REGISTER	0x0438~0x043C	HARD & SOFT
PORT4 VLAN CONTROL REGISTER	0x0440~0x0444	HARD & SOFT
PORT5 VLAN CONTROL REGISTER	0x0448~0x044C	HARD & SOFT
PORT6 VLAN CONTROL REGISTER	0x0450~0x0454	HARD & SOFT

3.5.1 ACL_FUNC0

Address 0x0400

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Table 3-82 summarizes the *ACL_FUNC0* Register 0

Table 3-82. **ACL Function Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	ACL_BUSY	DEPEND:ACL_DONE_INT, ACL table busy. This bit must be set to 1'b1 to start a ACL operation and cleared to zero after operation done. If this bit is set to 1'b1, CPU can't request another operation.
30:11	R/W	0	RESERVED	
10	R/W	0	ACL_FUNC	1'b0: write, 1'b1:read
9:8	R/W	0	ACL_RULE_SEL	2'b00: rule; 2'b01: mask; 2'b10:result; 2'b11:RESERVED ACL rule index
7	R/W	0	RESERVED	ACL rule index
6:0	R/W	0	ACL_FUNC_INDEX	ACL rule index

3.5.2 ACL_FUNC1

Address 0x0404

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Table 3-83 summarizes the ACL_FUNC1 Register

Table 3-83. **ACL Function Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W W	0	ACL_RULE_DATA_0	The ACL rule: byte [3:0]

3.5.3 ACL_FUNC2

Address 0x0408

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Table 3-84 summarizes the ACL_FUNC2 Register 2

Table 3-84. **ACL Function Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W W	0	ACL_RULE_DATA_1	The ACL rule: byte [7:4]

3.5.4 ACL_FUNC3

Address 0x040C

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Table 3-85 summarizes the ACL_FUNC3 Register 3

Table 3-85. **ACL Function Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W W	0	ACL_RULE_DATA_2	The ACL rule: byte [11:8]

3.5.5 ACL_FUNC4

Address 0x0410

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Table 3-86 summarizes the ACL_FUNC4 Register 4

Table 3-86. **ACL Function Register 4**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W W	0	ACL_RULE_DATA_3	The ACL rule: byte [15:12]

3.5.6 ACL_FUNC5

Address 0x0414

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Table 3-87 summarizes the ACL_FUNC5 Register 5

Table 3-87. **ACL Function Register 5**

Bit	R/W	Inital Value	Mnemonic	Description
31:8	R/W	0	RESERVED	
7:0	R/W	0	ACL_RULE_DATA_4	The ACL rule: byte [16]

3.5.7 PRIVATE_IP_CTRL

Address 0x0418

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Table 3-88 summarizes the PRIVATE_IP_CTRL Register

Table 3-88. **Private Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	RESERVED	
30	R/O	0	RESERVED	
29	R/O	0	RESERVED	
28	R/W	0	PRIVATE_IP_BASE_SEL	1'b1:{ip[31:20],ip[15:8]} 1'b0: ip[31:12]
27:20	R/O	0	RESERVED	
19:0	R/W	2'hC0A80	PRIVATE_IP_BASE_ADDR	Private ip base address

3.5.8 PORT0_VLAN_CTRL0

Address 0x0420

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Table 3-89 summarizes the PORT0_VLAN_CTRL0 Register 0

Table 3-89. **Port 0 Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_0	Port default cvlan priority for received frames.
28	R/O	0	RESERVED	
27:16	R/O	0x1	PORT_DEFAULT_CVID_0	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_0	Port default svlan priority for received frames.
12	R/O	0	RESERVED	
11:0	R/W	0x1	PORT_DEFAULT_SVID_0	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.

3.5.9 PORT0_VLAN_CTRL1

Address 0x0424

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Table 3-90, "Port 0 Control Register 1," on page 112 summarizes the PORT0_VLAN_CTRL1 Register 1

Table 3-90. **Port 0 Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:15	R/O	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_0	1'b0: all frames can be sent out. 1'b1: only tagged frames can be sent out.
13:12	R/W	0	EG_VLAN_MODE_0	Egress VLAN mode. 2'b00: egress should transmit frames unmodified. 2'b01: egress should transmit frames without VLAN 2'b10: egress should transmit frames with VLAN 2'b11:untouched
11	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
10	R/O	0	SPCHECK_EN_0	1'b1:L3 Source port check enable
9	R/W	0	CORE_PORT_EN_0	1'b1: core port; 1'b0: edge port
8	R/W	0	FORCE_DEFAULT_VID_EN_0	1'b1: force to use port default VID and priority for received frame, when 802.1Q mode is not disable. 1'b0: use frame tag only.
7	R/W	0	PORT_TLS_MODE_0	1'b1: port work at TLS mode 1'b0: port work at NON-TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_0	1'b1: enable port base vlan propagate function.
5	R/W	0	PORT_CLONE_EN_0	1'b1: enable port clocne. 1'b0: enable port replace
4	R/W	0	VLAN_PRI_PRO_EN_0	1.b1: vlan priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_0	2'b00: all frame can be received in, include untagged and tageed. 2'b01: only frame with tag can be received by this port. 2'b10: only frame untagged can be received by this port, include no vlan and priority vlan. 2'b11: reserved for future.
1:0	R/O	0	RESERVED	

3.5.10 PORT1_VLAN_CTRL0

Address 0x0428

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Table 3-91 summarizes the PORT1_VLAN_CTRL0 Register

Table 3-91. **Port 1 Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_1	Port default cvlan priority for received frames.
28	R/O	0	RESERVED	
27:16	R/W	0X1	PORT_DEFAULT_CVID_1	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	1	ING_PORT_SPRI_1	Port default svlan priority for received frames.
12	R/O	0	RESERVED	
11:0	R/W	0X1	PORT_DEFAULT_SVID_1	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.

3.5.11 PORT1_VLAN_CTRL1

Address 0x042C

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Table 3-92 summarizes the PORT1_VLAN_CTRL1 Register 1

Table 3-92. **Port 1 VLAN Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:15	R/O	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_1	1'b0: all frames can be sent out. 1'b1: only tagged frames can be sent out.
13:12	R/W	0	EG_VLAN_MODE_1	Egress VLAN mode. 2'b00: egress should transmit frames unmodified. 2'b01: egress should transmit frames without VLAN 2'b10: egress should transmit frames with VLAN 2'b11:untouched
11	R/O	0	RESERVED	
10	R/W	0	SPCHECK_EN_1	1'b1:L3 Source port check enable

Bit	R/W	Inital Value	Mnemonic	Description
9	R/W	0	CORE_PORT_EN_1	1'b1: core port; 1'b0: edge port
8	R/W	0	FORCE_DEFAULT_VID_EN_1	1'b1: force to use port default VID and priority for received frame, when 802.1Q mode is not disable. 1'b0: use frame tag only.
7	R/W	0	PORT_TLS_MODE_1	1'b1: port work at TLS mode 1'b0: port work at NON-TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_1	1'b1: enable port base vlan propagate function.
5	R/W	0	PORT_CLONE_EN_1	1'b1: enable port clocne. 1'b0: enable port replace
4	R/W	0	VLAN_PRI_PRO_EN_1	1.b1: vlan priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_1	2'b00: all frame can be received in, include untagged and tageed. 2'b01: only frame with tag can be received by this port. 2'b10: only frame untagged can be received by this port, include no vlan and priority vlan. 2'b11: reserved for future.
0	R/O	0	RESERVED	

3.5.12 PORT2_VLAN_CTRL0

Address 0x0430

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Table 3-93 summarizes the PORT2_VLAN_CTRL0 Register 0

Table 3-93. **Port 2 VLAN Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_2	Port default cvlan priority for received frames.
28	R/O	0	RESERVED	
27:16	R/W	0X1	PORT_DEFAULT_CVID_2	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_2	Port default svlan priority for received frames.
12	R/O	0	RESERVED	
11:0	R/W	0X1	PORT_DEFAULT_SVID_2	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.

3.5.13 PORT2_VLAN_CTRL1

Address 0x0434

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Table 3-94 summarizes the PORT2_VLAN_CTRL1 Register 1

Table 3-94. **Port 2 VLAN Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:15	R/O	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_2	1'b0: all frames can be sent out. 1'b1: only tagged frames can be sent out.
13:12	R/W	0	EG_VLAN_MODE_2	Egress VLAN mode. 2'b00: egress should transmit frames unmodified. 2'b01: egress should transmit frames without VLAN 2'b10: egress should transmit frames with VLAN 2'b11:untouched
11	R/O	0	RESERVED	
10	R/W	0	SPCHECK_EN_2	1'b1:L3 Source port check enable
9	R/W	0	CORE_PORT_EN_2	1'b1: core port; 1'b0: edge port
8	R/W	0	FORCE_DEFAULT_VID_EN_2	1'b1: force to use port default VID and priority for received frame, when 802.1Q mode is not disable. 1'b0: use frame tag only.
7	R/W	0	PORT_TLS_MODE_2	1'b1: port work at TLS mode 1'b0: port work at NON-TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_2	1'b1: enable port base vlan propagate function.
5	R/W	0	PORT_CLONE_EN_2	1'b1: enable port clocne. 1'b0: enable port replace
4	R/W	0	VLAN_PRI_PRO_EN_2	1.b1: vlan priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_2	2'b00: all frame can be received in, include untagged and tageed. 2'b01: only frame with tag can be received by this port. 2'b10: only frame untagged can be received by this port, include no vlan and priority vlan. 2'b11: reserved for future.
0	R/O	0	RESERVED	

3.5.14 PORT3_VLAN_CTRL0 Address 0x0438

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Table 3-95 summarizes the PORT3_VLAN_CTRL0 Register 0

Table 3-95. **Port 3 VLAN Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_3	Port default cvlan priority for received frames.
28	R/O	0	RESERVED	
27:16	R/W	0X1	PORT_DEFAULT_CVID_3	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_3	Port default svlan priority for received frames.
12	R/O	0	RESERVED	
11:0	R/W	0X1	PORT_DEFAULT_SVID_3	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.

3.5.15 PORT3_VLAN_CTRL1

Address 0x043C

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Table 3-96 summarizes the PORT3_VLAN_CTRL1 Register 1

Table 3-96. **Port 3 VLAN Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:15	R/O	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_3	1'b0: all frames can be sent out. 1'b1: only tagged frames can be sent out.
13:12	R/W	0	EG_VLAN_MODE_3	Egress VLAN mode. 2'b00: egress should transmit frames unmodified. 2'b01: egress should transmit frames without VLAN 2'b10: egress should transmit frames with VLAN 2'b11:untouched
11	R/O	0	RESERVED	
10	R/W	0	SPCHECK_EN_3	1'b1:L3 Source port check enable

Bit	R/W	Inital Value	Mnemonic	Description
9	R/W	0	CORE_PORT_EN_3	1'b1: core port; 1'b0: edge port
8	R/W	0	FORCE_DEFAULT_VID_EN_3	1'b1: force to use port default VID and priority for received frame, when 802.1Q mode is not disable. 1'b0: use frame tag only.
7	R/W	0	PORT_TLS_MODE_3	1'b1: port work at TLS mode 1'b0: port work at NON-TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_3	1'b1: enable port base vlan propagate function.
5	R/W	0	PORT_CLONE_EN_3	1'b1: enable port clocne. 1'b0: enable port replace
4	R/W	0	VLAN_PRI_PRO_EN_3	1.b1: vlan priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_3	2'b00: all frame can be received in, include untagged and tageed. 2'b01: only frame with tag can be received by this port. 2'b10: only frame untagged can be received by this port, include no vlan and priority vlan. 2'b11: reserved for future.
0	R/O	0	RESERVED	

3.5.16 PORT4_VLAN_CTRL0

Address 0x0440

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Table 3-97 summarizes the PORT4_VLAN_CTRL0 Register 0

Table 3-97. **Port 4 VLAN Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_4	Port default cvlan priority for received frames.
28	R/O	0	RESERVED	
27:16	R/W	0X1	PORT_DEFAULT_CVID_4	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_4	Port default svlan priority for received frames.
12	R/O	0	RESERVED	
11:0	R/W	0X1	PORT_DEFAULT_SVID_4	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.

3.5.17 PORT4_VLAN_CTRL1

Address 0x0444

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Table 3-98 summarizes the PORT4_VLAN_CTRL1 Register 1

Table 3-98. **Port 4 VLAN Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:15	R/O	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_4	1'b0: all frames can be sent out. 1'b1: only tagged frames can be sent out.
13:12	R/W	0	EG_VLAN_MODE_4	Egress VLAN mode. 2'b00: egress should transmit frames unmodified. 2'b01: egress should transmit frames without VLAN 2'b10: egress should transmit frames with VLAN 2'b11:untouched
11	R/O	0	RESERVED	
10	R/W	0	SPCHECK_EN_4	1'b1:L3 Source port check enable
9	R/W	0	CORE_PORT_EN_4	1'b1: core port; 1'b0: edge port
8	R/W	0	FORCE_DEFAULT_VID_EN_4	1'b1: force to use port default VID and priority for received frame, when 802.1Q mode is not disable. 1'b0: use frame tag only.
7	R/W	0	PORT_TLS_MODE_4	1'b1: port work at TLS mode 1'b0: port work at NON-TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_4	1'b1: enable port base vlan propagate function.
5	R/W	0	PORT_CLONE_EN_4	1'b1: enable port clocne. 1'b0: enable port replace
4	R/W	0	VLAN_PRI_PRO_EN_4	1.b1: vlan priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_4	2'b00: all frame can be received in, include untagged and tageed. 2'b01: only frame with tag can be received by this port. 2'b10: only frame untagged can be received by this port, include no vlan and priority vlan. 2'b11: reserved for future.
0	R/O	0	RESERVED	

3.5.18 PORT5_VLAN_CTRL0

Address 0x0448

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Table 3-99 summarizes the PORT5_VLAN_CTRL0 Register 0

Table 3-99. **Port 5 VLAN Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_5	Port default cvlan priority for received frames.
28	R/O	0	RESERVED	
27:16	R/W	0X1	PORT_DEFAULT_CVID_5	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_5	Port default svlan priority for received frames.
12	R/O	0	RESERVED	
11:0	R/W	0X1	PORT_DEFAULT_SVID_5	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.

3.5.19 PORT5_VLAN_CTRL1

Address 0x044C

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Table 3-100 summarizes the PORT5_VLAN_CTRL1 Register 1

Table 3-100. **Port 5 VLAN Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:15	R/O	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_5	1'b0: all frames can be sent out. 1'b1: only tagged frames can be sent out.
13:12	R/W	0	EG_VLAN_MODE_5	Egress VLAN mode. 2'b00: egress should transmit frames unmodified. 2'b01: egress should transmit frames without VLAN 2'b10: egress should transmit frames with VLAN 2'b11:untouched
11	R/O	0	RESERVED	
10	R/W	0	SPCHECK_EN_5	1'b1:L3 Source port check enable

Bit	R/W	Inital Value	Mnemonic	Description
9	R/W	0	CORE_PORT_EN_5	1'b1: core port; 1'b0: edge port
8	R/W	0	FORCE_DEFAULT_VID_EN_5	1'b1: force to use port default VID and priority for received frame, when 802.1Q mode is not disable. 1'b0: use frame tag only.
7	R/W	0	PORT_TLS_MODE_5	1'b1: port work at TLS mode 1'b0: port work at NON-TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_5	1'b1: enable port base vlan propagate function.
5	R/W	0	PORT_CLONE_EN_5	1'b1: enable port clocne. 1'b0: enable port replace
4	R/W	0	VLAN_PRI_PRO_EN_5	1.b1: vlan priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_5	2'b00: all frame can be received in, include untagged and tageed. 2'b01: only frame with tag can be received by this port. 2'b10: only frame untagged can be received by this port, include no vlan and priority vlan. 2'b11: reserved for future.
0	R/O	0	RESERVED	

3.5.20 PORT6_VLAN_CTRL0

Address 0x0450

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Table 3-101 summarizes the PORT6_VLAN_CTRL0 Register 0

Table 3-101. **Port 6 VLAN Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_6	Port default cvlan priority for received frames.
28	R/O	0	RESERVED	
27:16	R/W	0X1	PORT_DEFAULT_CVID_6	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_6	Port default svlan priority for received frames.
12	R/O	0	RESERVED	
11:0	R/W	0X1	PORT_DEFAULT_SVID_6	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.

3.5.21 PORT6_VLAN_CTRL1

Address 0x0454

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Table 3-102 summarizes the PORT6_VLAN_CTRL1 Register 1

Table 3-102. **Port 6 VLAN Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:15	R/O	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_6	1'b0: all frames can be sent out. 1'b1: only tagged frames can be sent out.
13:12	R/W	0	EG_VLAN_MODE_6	Egress VLAN mode. 2'b00: egress should transmit frames unmodified. 2'b01: egress should transmit frames without VLAN 2'b10: egress should transmit frames with VLAN 2'b11:untouched
11	R/O	0	RESERVED	
10	R/W	0	SPCHECK_EN_6	1'b1:L3 Source port check enable
9	R/W	0	CORE_PORT_EN_6	1'b1: core port; 1'b0: edge port
8	R/W	0	FORCE_DEFAULT_VID_EN_6	1'b1: force to use port default VID and priority for received frame, when 802.1Q mode is not disable. 1'b0: use frame tag only.
7	R/W	0	PORT_TLS_MODE_6	1'b1: port work at TLS mode 1'b0: port work at NON-TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_6	1'b1: enable port base vlan propagate function.
5	R/W	0	PORT_CLONE_EN_6	1'b1: enable port clocne. 1'b0: enable port replace
4	R/W	0	VLAN_PRI_PRO_EN_6	1.b1: vlan priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_6	2'b00: all frame can be received in, include untagged and tageed. 2'b01: only frame with tag can be received by this port. 2'b10: only frame untagged can be received by this port, include no vlan and priority vlan. 2'b11: reserved for future.
0	R/O	0	RESERVED	

3.5.22 IPv6 Private Base Address Register 0 Address: 0x0470

Table 3-103 summarizes the IPv6 Private base address register 0.

Table 3-103. **IPv6 Private Base Address Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W	0	IPV6_PRIVATE_IP0	IPv6 private base address 0 The 96-bit IPv6 private address is split and stored into three registers—{IP2, IP1 and IP0}

3.5.23 IPv6 Private Base Address Register 1

Address: 0x0474

Table 3-104 summarizes the IPv6 Private base address register 1.

Table 3-104. **IPv6 Private Base Address Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W	0	IPV6_PRIVATE_IP1	IPv6 private base address 1 The 96-bit IPv6 private address is split and stored into three registers—{IP2, IP1 and IP0}

3.5.24 IPv6 Private Base Address Register 2

Address: 0x0478

Table 3-105 summarizes the IPv6 Private base address register 2.

Table 3-105. **IPv6 Private Base Address Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W	0	IPV6_PRIVATE_IP2	IPv6 private base address 2 The 96-bit IPv6 private address is split and stored into three registers—{IP2, IP1 and IP0}

3.6 LOOKUP REGISTER (Address Range: 0x0600 ~ 0x0708)

Table 3-106 summarizes the registers.

Table 3-106. **Parser Register Summary**

Name	Address	Reset
ATU FUNCTION REGISTER	0x0600~0x060C	HARD & SOFT
VTU FUNCTION REGISTER	0x0610~0x0614	HARD & SOFT
ARL CONTROL REGISTER	0x0618	HARD & SOFT
GLOBAL FORWARD CONTROL REGISTER	0x0620~0x0624	HARD & SOFT
GLOBAL LEARN LIMIT CONTROL	0x0028	HARD & SOFT
TOS TO PRI MAP REGISTER	0x0630~0x064C	HARD & SOFT
VLAN PRI TO PRI MAP REGISTER	0x0650	HARD & SOFT
LOOP CHECK RESULT	0x0654	HARD & SOFT
PORT0 LOOKUP CONTROL REGISTER	0x0660	HARD & SOFT
PORT0 PRIORITY CONTROL REGISTER	0x0664	HARD & SOFT
PORT0 LEARN LIMIT CONTRL REGISTER	0x0668	HARD & SOFT
PORT1 LOOKUP CONTROL REGISTER	0x066C	HARD & SOFT
PORT1 PRIORITY CONTROL REGISTER	0x0670	HARD & SOFT
PORT1 LEARN LIMIT CONTRL REGISTER	0x0674	HARD & SOFT
PORT2 LOOKUP CONTROL REGISTER	0x0678	HARD & SOFT
PORT2 PRIORITY CONTROL REGISTER	0x067C	HARD & SOFT
PORT2 LEARN LIMIT CONTRL REGISTER	0x0680	HARD & SOFT
PORT3 LOOKUP CONTROL REGISTER	0x0684	HARD & SOFT
PORT3 PRIORITY CONTROL REGISTER	0x0688	HARD & SOFT
PORT3 LEARN LIMIT CONTRL REGISTER	0x068C	HARD & SOFT
PORT4 LOOKUP CONTROL REGISTER	0x0690	HARD & SOFT
PORT4 PRIORITY CONTROL REGISTER	0x0694	HARD & SOFT
PORT4 LEARN LIMIT CONTRL REGISTER	0x0698	HARD & SOFT
PORT5 LOOKUP CONTROL REGISTER	0x069C	HARD & SOFT
PORT5 PRIORITY CONTROL REGISTER	0x06A0	HARD & SOFT
PORT5 LEARN LIMIT CONTRL REGISTER	0x06A4	HARD & SOFT
PORT6 LOOKUP CONTROL REGISTER	0x06A8	HARD & SOFT
PORT6 PRIORITY CONTROL REGISTER	0x06AC	HARD & SOFT
PORT6 LEARN LIMIT CONTRL REGISTER	0x06B0	HARD & SOFT
Trunk Control Registers		
TRUNK CONTROL0 REGISTER	0x0700	HARD & SOFT
TRUNK CONTROL1 REGISTER	0x0704	HARD & SOFT
TRUNK CONTROL2 REGISTER	0x0708	HARD & SOFT

3.6.1 ATU_DATA0

Address 0x0600

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Table 3-107 summarizes the ATU_DATA0 Register 0

Table 3-107. **ATU DATA 0 Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W W	0	ATU_MAC_ADDR0	this is the MAC address bit [31:0]

3.6.2 ATU_DATA1

Address 0x0604

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Table 3-108 summarizes the ATU_DATA1 Register 1

Table 3-108. **ATU DATA 1 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W W	0	ATU_HASH_HIGH_ADDR	Mac hash addr max bit use for get next
30	R/W W	0	ATU_SA_DROP_EN	Drop packet enable when source address is in this entry. If this bit is set to 1'b1, the packet with sa of this entry will be dropped.
29	R/W W	0	ATU_MIRROR_EN	1: indicates packets should be send to mirror port and destination port. 0: indicates packets should only be send to destination port.
28	R/W W	0	ATU_PRI_OVER_EN	Priority override enable. 1: indicates ATU_PRI can override any other priority determined by the frame's data.
27	R/W W	0	ATU_SVL_ENTRY	1'b1: SVL learned; 1'b0: IVL learned
26:24	R/W W	0	ATU_PRI	This priority bits may be used as frame's priority when PRI_OVER_EN set to one.
23	R/W W	0	ATU_CROSS_PORT_STATE_EN	1'b1, cross port_state enable
22:16	R/W W	0	ATU_DES_PORT	These bits indicate which ports are associated with this mac address when they are set to one. Bit 16 is assigned to port0, 17 to port1, 18 to port2,etc
15:0	R/W W	0	ATU_MAC_ADDR1	mac address bit [47:32]

3.6.3 ATU_DATA2

Address 0x0608

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Table 3-109 summerizes the ATU_DATA2 Register

Table 3-109. **ATU_DATA2 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:20	R/W	0	RESERVED	
19:8	R/W	0	ATU_VID	This MAC address is the member of ATU_VID group.
7	R/W	0	ATU_SHORT_LOOP	If learn engine find source port mismatch then set to 1, loopcheck engine clear it
6	R/W	0	ATU_COPY_TO_CPU	1'b1: packet received with this address should be copied to cpu port.
5	R/W	0	ATU_REDIRECT_TO_CPU	1'b1: packet received with this address should be redirected to cpu port. If no cpu connected to switch, this frame should be discarded.
4	R/W	0	ATU_LEAKY_EN	1'b1: use leaky VLAN enable for this mac address This bit can be used for unicast and multicast frame, control by ARL_uni_leaky_en and ARL_multi_leaky_en
3:0	R/W	0	ATU_STATUS	4'h0:indicates entry is empty 4'h1~7:indicates entry is dynamic and valid. 4'h8~4'hE: entry is dynamic and valid, can be age but can't be changed by any other address. 4'hF:indicates entry is static and won't be age or change by hardware.

3.6.4 ATU_FUNC_REG

Address 0x060C

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Table 3-110 summerizes the ATU_FUNC_REG Register

Table 3-110. **ATU_FUNC_REG Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W SC	0	AT_BUSY	DEPEND: AT_DONE, Address table busy. This bit must be set to 1'b1 to start an AT operation and cleared to zero by hardware after the operation is done. If this bit is 1'b1 on read, cpu can't request another operation.
30:25	R/O	0	RESERVED	
24:22	R/W	0	TRUNK_PORT_NUM	TRUNK port number. When CPU function is "CHANGE TRUNK PORT", the AT_PORT_NUM in arl bitmap will be changed to TRUNK_PORT_NUM.
21	R/O	0	RESERVED	
20:16	R/W	0	ATU_INDEX	If ATU_TYPE is reserved ATU Entry, this index is the address of Reserved ATU entry
15	R/W	0	AT_VID_EN	1'b1: when CPU function is "GET NEXT", the vid in the valid ARL entry must be equal to the vid we set
14	R/W	0	AT_PORT_EN	1'b1: when CPU function is "GET NEXT", the AT_PORT_NUM must be in the Destination port in the valid ARL entry.
13	R/W	0	AT_MULTI_EN	1'b1: when CPU function is "GET NEXT", the high bytes of mac address in the valid ARL entry must be 0x01005E or 0x3333. 1'b0: all enty
12	R/W	0	AT_FULL_VIO	ARL table full violation. This bit is set to 1'b1 if the ARL table is full when cpu want to add a new entry to ARL table, and also be set to 1'b1 if the ARL table is empty when cpu want to purge an entry to ARL table.
11:8	R/W	0	AT_PORT_NUM	Port number to be flushed. If "AT_FUNC" is set to 4'b0101, lookup module must flush all unicast entries for the port.(or flush the port from ARL table)
7:6	R/O	0	RESERVED	
5	R/W	0	ATU_TYPE	1'b1:Reserved ATU Entry 1'b0: Normal ATU Entry.

Bit	R/W	Inital Value	Mnemonic	Description
4	R/W	0	FLUSH_STATIC_EN	1'b1: when AT_FUNC set to 3'b101, static entry in arl table can be flush. 1'b0: when AT_FUNC set to 3'b101, only flush dynamic entry in ARL table.
3:0	R/W	0	AT_FUNC	Address table operate function. 4'b0000: No operation. 4'b0001: Flush all entries. 4'b0010: load an entry. If these bits are set to 3'b010, cpu want to load an entry into ARL table. 4'b0011: purge an entry. If these bits are set to 3'b011, cpu want to purge an entry from ARL table. 4'b0100: flush all unlocked entries in ARL. 4'b0101: flush one port from arl table 4'b0110: get next valid or static entry in ARL table. If address and at_status and vid are all zero, hardware will search the first valid entry from entry0. If address is set to zero and at_status is not zero, hardware will search next valid entry from entry which address is 48'h0. If hardware return back with address and at_status and vid all zero, there's no other next valid entry in ARL table. 4'b0111: search mac address 4'b1000: change trunk port

3.6.5 VTU_FUNC_REG0

Address 0x0610

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Table 3-111 summerizes the VTU_FUNC_REG0 Register

Table 3-111. **VTU_FUNC_REG0 Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:21	R/O	0	RESERVED	
20	R/W W	0	VTU_VALID	1:indicates entry is valid 0:indicates entry is empty
19	R/W W	0	VTU_IVL_EN	1:indicates this vid is used to ivl 0:indicates this vid is used to svl, vid replaced by 0 when search mac address.

Bit	R/W	Inital Value	Mnemonic	Description
18	R/W W	0	VTU_LEARN_LOOKUP_DIS	1:indicates no learn and not use arl table DP calculate final DP, but use uni flood DP as ARL DP to calculate DP 0:indicates normal operation about learn and final DP
17:4	R/W W	0	VTU_EG_VLAN_MODE	5:4 for port0, 7:6 for port1 …17:16 for port6 2'b00: unmodified 2'b01: untagged 2'b10: tagged 2'b11: not member
3	R/W W	0	VTU_PRI_OVER_EN	VLAN Priority override enable.
2:0	R/W W	0	VTU_PRI	This priority bits may be used as frame's priority when VTU_PRI_OVER_EN set to one.

3.6.6 VTU_FUNC_REG1

Address 0x0614

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Table 3-112 summerizes the VTU_FUNC_REG1 Register 1

Table 3-112. **VTU Function Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W SC	0	VT_BUSY	DEPEND:VT_DONE, VLAN table busy. This bit must be set to 1'b1 to start a VT operation and cleared to zero after operation done. If this bit is set to 1'b1, cpu can't request another operation.
30:28	R/O	0	RESERVED	
27:16	R/W W	0	VID	DEPEND:VT_DONE,VT_CSR_VID[11:0], Value of VLAN ID to be added or purged.
15:12	R/O	0	RESERVED	
11:8	R/W	0	VT_PORT_NUM	Port number.
7:5	R/O	0	RESERVED	
4	R/O C	0	VT_FULL_VIO	VLAN table full violation. This bit is set to 1'b1 if the VLAN table is full when cpu want to add a new VID to VLAN table.

Bit	R/W	Inital Value	Mnemonic	Description
3	R/O	0	RESERVED	
2:0	R/W	0	VT_FUNC	VLAN table operate function. 3'b000: No operation. 3'b001: Flush all entries. 3'b010: load an entry. If these bits are set to 3'b010, cpu want to load an entry into VLAN table. 3'b011: purge an entry. If these bits are set to 3'b011, cpu want to purge an entry from VLAN table. 3'b100:remove an port from VLAN table. The port number which need to be removed is indicated in VT_PORT_NUM. 3'b101:get next If vid is 12'b0 and vt_busy is set by software, hardware should search the first valid entry in VLAN table. If vid is 12'b0and vt_busy is reset by hard ware, there's no valid entry from VID set by software. 3'b110: read one entry

3.6.7 ARL_CTRL

Address 0x00618

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Table 3-113 summerizes the ARL_CTRL Register

Table 3-113. **ARL Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W SC	0	RESERVED	
30	R/W	1'b0	LEARN_CHANGE_EN	1'b1: enable new mac address change old one if hash violation occur when learning 1'b0: if hash violation occur when learning, no new address be learned to arl.
29	R/W	1'b0	IGMP_JOIN_LEAKY_EN	Igmp join address leaky vlan enable. 1'b1: igmp join address should be set to leaky_en in ARL table, bit 68 in ATU entry is set to 1'b1. 1'b0: igmp join address needn't be set to leaky_en in ARL table, bit 68 in ATU entry is set to 1'b0.
28	R/W	0	IGMP_JOIN_NEW_EN	1'b1: enable hardware add new address to ARL table when received IGMP/MLD join frame, and remove address from ARL when received IGMP/MLD leave frame.
27	R/W	1'b0	IGMP_JOIN_PRI_REMAP_EN	Use for igmp packet learn in arl table, define DA priority remap enable (atu[60])

Bit	R/W	Inital Value	Mnemonic	Description
26:24	R/W	3'b0	IGMP_JOIN_PRI	Use for igmp packet learn in arl table, define DA priority (atu[59:57)
23:20	R/W	4'hF	IGMP_JOIN_STATUS	Use for igmp packet learn in arl table, define the status (atu[67:64])
19	R/W	1'b1	AGE_EN	Enable age operation. 1'b1: lookup module can age the address in the address table.
18:16	R/W	0	LOOP_CHECK_TIMER	3'h0: disable loop back check 3'h1: 1ms 3'h2: 10ms 3'h3: 100ms 3'h4: 500ms 3'h5~7: reserved
15:0	R/W	'h2B	AGE_TIME	Address Table Age Timer. These bits determine the time that each entry remains valid in the address table, since last accessed. For the time is times 7s, maximum age time is about 10,000 minutes. The default value is 'h2B for five minutes. If AGE_EN is set to 1'b1, these bits shouldn't be set to zero.

3.6.8 GLOBAL_FW_CTRL0

Address 0x0620

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Table 3-114 summerizes the GLOBAL_FW_CTRL0 Register

Table 3-114. **Global Forward Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27:26	R/W	0	ARP_FORWARD_ACT	0:REDIRECT TO CPU 1:COPY TO CPU 2:FORWARD
25:24	R/W	0	SP_NOT_FOUND_ACT	For IP packet 0:FORWARD 1:DROP 2:TO CPU
23:22	R/W	0	ARP_SP_NOT_FOUND_ACT	For ARP packet 0:FORWARD 1:DROP 2:TO CPU
21:20	R/W	0	HASH_MODE	Hash mode for Mac address. 0: crc_16, 1: crc_10

Bit	R/W	Inital Value	Mnemonic	Description
19	R/W	0	ARP_REQ_UNI	
18	R/O	0	RESERVED	
17	R/W	0	NAT_NOT_FOUND_DROP_EN	1'b1: drop 1'b0: to cpu
16	R/O	0	RESERVED	
15	R/O	0	RESERVED	
14	R/W	0	IGMP_LEAVE_DROP_EN	IGMP/MLD leave packet. After updated the portmap of ARL(IGMP/MLD Group address). If portmap in ARL is not empty, 1'b1: drop this packet. 1'b0: forwarding to IGMP_JOIN_LEAVE_DP
13	R/W	0	ARL_UNI_LEAKY_EN	1'b1: use LEAKY_EN bit in ARL table to control unicast frame leaky VLAN, and ignore "UNI_LEAKY_EN". 1'b0: ignore LEAKY_EN bit in ARL table to control unicast frame leaky VLAN. Only use port base UNI_LEAKY_EN to control unicast frame leaky VLAN.
12	R/W	0	ARL_MULTI_LEAKY_EN	1'b1: use LEAKY_EN bit in ARL table to control multicast frame leaky VLAN, and ignore "MULTI_LEAKY_EN". 1'b0: ignore LEAKY_EN bit in ARL table to control multicast frame leaky VLAN. Only use port base MULTI_LEAKY_EN to control multicast frame leaky VLAN.
11	R/W	1	MANAGE_VID_VIO_DROP_EN	1'b1: management frame should be drop if vlan violation occur 1'b0: management frame transmit out if vlan violation occur.
10	R/W	0	CPU_PORT_EN	1''b1: cpu is connected to port0; 1'b0: no cpu connect to switch If this bit is set to 1'b1, head_en of mac0 should be set to 1'b1.
9	R/O	1'b0	RESERVED	
8	R/W	1'b0	PPPOE_REDIRECT_EN	PPPoE discovery frame redirect to cpu enable. If this bit is set to 1'b1, PPPoE discovery frame should be redirect to cpu port. If this bit set to 1'b0, PPPoE discovery frame should be tranmit as normal frame.
7:4	R/W	0xF	MIRROR_PORT_NUM	Port number which packet should be mirrored to. 4'h0 is port0, 4'h1 is port1,etc. If value more than 6, no mirror port connected to switch

Bit	R/W	Inital Value	Mnemonic	Description
3	R/W	0	IGMP_COPY_EN	1'b1: qm should copy IGMP/MLD frame to cpu port. 1'b0: qm should redirect IGMP/MLD frame to cpu port. This IGMP not include the IGMP JOIN/ LEAVE packet
2	R/W	1'b0	RIP_COPY_EN	1'b1 : rip v1 frame copy to cpu 1'b0: don't copy rip v1 frame to cpu
1	R/W	0	RESERVED	
0	R/W	1'b0	EAPOL_REDIRECT_EN	1'b1:802.1x frame redirect to cpu 1'b0: 802.1x frame copy to cpu

3.6.9 GLOBAL_FW_CTRL1

Address 0x0624

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Table 3-115 summarizes the GLOBAL_FW_CTRL1 Register 1

Table 3-115. **Global Forward Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	Reserved	
30:24	R/W	0	IGMP_JOIN_LEAVE_DP	If mac receive IGMP/MLD fast join or leave frame, should be send due to these bits map destination port. Notes: cpu port can cross vlan if port bit map set to 1'b1.
23	R/W	0	RESERVED	
22:16	R/W	7'h7E	BROAD_DP	If mac received broadcast frame use these bits to determine destination port.
15	R/O	0	RESERVED	
14:8	R/W	7'h7E	MULTI_FLOOD_DP	If mac received unknown multicast frame which DA is not contained in ARL table, use these bits to determine destination port.
7	R/0	0	RESERVED	
6:0	R/W	7'h7E	UNI_FLOOD_DP	If mac received unknown unicast frame which DA is not contained in ARL table, use these bits to determine destination port.

3.6.10 GOL_LEARN_LIMIT

Address 0x0628

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Table 3-116 summarizes the GOL_LEARN_LIMIT Register

Table 3-116. **Global Learn Limit Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:13	R/O	0	RESERVED	
12	R/W	0	GOL_SA_LEARN_LIMIT_EN	1'b1: SA Learn Limit enable.
11	R/W	0	GOL_SA_LEARN_LIMIT_DROP_EN	1'b1: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to GOL_SA_LEARN_CNT 1'b0: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to GOL_SA_LEARN_CNT
10:0	R/W	0	GOL_SA_LEARN_CNT	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: indicates no MAC limit number is 1 1: indicates the MAC limit number is 2 2: indicates the MAC limit number is 3 ... and so on ... until: 2047: indicates the MAC limit is 2048

3.6.11 TOS_PRI_MAP_REG0

Address 0x0630

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Table 3-117 summarizes the TOS_PRI_MAP_REG0 Register 0

Table 3-117. **TOS Priority Mapping Register Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0X1C	See bit 3:0
27:24	R/W	0	TOS_MAP_0X18	See bit 3:0
23:20	R/W	0	TOS_MAP_0X14	See bit 3:0
19:16	R/W	0	TOS_MAP_0X10	See bit 3:0
15:12	R/W	0	TOS_MAP_0X0C	See bit 3:0
11:8	R/W	0	TOS_MAP_0X08	See bit 3:0

Bit	R/W	Inital Value	Mnemonic	Description
7:4	R/W	0	TOS_MAP_0X04	3:0 DEI
3:0	R/W	0	TOS_MAP_0X00	2:0 PRIORITY

3.6.12 TOS_PRI_MAP_REG1

Address 0x0634

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Table 3-118 summarizes the TOS_PRI_MAP_REG1 Register 1

Table 3-118. **TOS/TC to Priority Mapping Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0X3C	See bit 3:0 of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0X38	See bit 3:0 of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0X34	See bit 3:0 of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0X30	See bit 3:0 of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0X2C	See bit 3:0 of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0X28	See bit 3:0 of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0X24	See bit 3:0 of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0X20	

3.6.13 TOS_PRI_MAP_REG2

Address 0x0638

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Table 3-119 summarizes the TOS_PRI_MAP_REG2 Register 2

Table 3-119. **TOS/TC to Priority Mapping Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0X5C	See bit 3:0 of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0X58	See bit 3:0 of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0X54	See bit 3:0 of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0X50	See bit 3:0 of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0X4C	See bit 3:0 of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0X48	See bit 3:0 of TOS_PRI_MAP_REG0

Bit	R/W	Inital Value	Mnemonic	Description
7:4	R/W	0	TOS_MAP_0X44	See bit 3:0 of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0X40	

3.6.14 TOS_PRI_MAP_REG3

Address 0x063C

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Table 3-120 summarizes the TOS_PRI_MAP_REG3 Register 3

Table 3-120. **TOS/TC to Priority Mapping Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0X7C	See bit 3:0 of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0X78	See bit 3:0 of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0X74	See bit 3:0 of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0X70	See bit 3:0 of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0X6C	See bit 3:0 of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0X68	See bit 3:0 of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0X64	See bit 3:0 of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0X60	See bit 3:0 of TOS_PRI_MAP_REG0

3.6.15 TOS_PRI_MAP_REG4

Address 0x0640

SFT&HW RST

Table 3-121 summarizes the TOS_PRI_MAP_REG4 Register 4

Table 3-121. **TOS/TC to Priority Mapping Register 4**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0X9C	See bit 3:0 of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0X98	See bit 3:0 of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0X94	See bit 3:0 of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0X90	See bit 3:0 of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0X8C	See bit 3:0 of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0X88	See bit 3:0 of TOS_PRI_MAP_REG0

Bit	R/W	Inital Value	Mnemonic	Description
7:4	R/W	0	TOS_MAP_0X84	See bit 3:0 of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0X80	See bit 3:0 of TOS_PRI_MAP_REG0

3.6.16 TOS_PRI_MAP_REG5

Address 0x0644

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page 137 summarizes the TOS_PRI_MAP_REG5 Register 5

Table 3-122. **TOS/TC to Priority Mapping Register 5**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0XBC	See bit 3:0 of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0XB8	See bit 3:0 of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0XB4	See bit 3:0 of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0XB0	See bit 3:0 of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0XAC	See bit 3:0 of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0XA8	See bit 3:0 of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0XA4	See bit 3:0 of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0XA0	See bit 3:0 of TOS_PRI_MAP_REG0

3.6.17 TOS_PRI_MAP_REG6

Address 0x0648

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Table 3-123, "TOS/TC to Priority Mapping Register 6," on page 137 summarizes the TOS_PRI_MAP_REG6 Register 6

Table 3-123. **TOS/TC to Priority Mapping Register 6**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0XDC	See bit 3:0 of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0XD8	See bit 3:0 of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0XD4	See bit 3:0 of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0XD0	See bit 3:0 of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0XCC	See bit 3:0 of TOS_PRI_MAP_REG0

Bit	R/W	Inital Value	Mnemonic	Description
11:8	R/W	0	TOS_MAP_0XC8	See bit 3:0 of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0XC4	See bit 3:0 of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0XC0	See bit 3:0 of TOS_PRI_MAP_REG0

3.6.18 TOS_PRI_MAP_REG7

Address 0x064C

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Table 3-124 summarizes the TOS_PRI_MAP_REG7 Register 7

Table 3-124. **TOS/TC to Priority Mapping Register 7**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0XFC	See bit 3:0 of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0XF8	See bit 3:0 of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0XF4	See bit 3:0 of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0XF0	See bit 3:0 of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0XEC	See bit 3:0 of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0XE8	See bit 3:0 of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0XE4	See bit 3:0 of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0XE0	See bit 3:0 of TOS_PRI_MAP_REG0

3.6.19 VLAN_PRI_MAP_REG0

Address 0x0650

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Table 3-125 sumarizes the VLAN_PRI_MAP_REG0 Register 0

Table 3-125. **VLAN Priority to Priority Mapping Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/W	7	VLAN_MAP_0X7	See bit 3:0 of VLAN_PRI_MAP_REG0
27:24	R/W	6	VLAN_MAP_0X6	See bit 3:0 of VLAN_PRI_MAP_REG0
23:20	R/W	5	VLAN_MAP_0X5	See bit 3:0 of VLAN_PRI_MAP_REG0
19:16	R/W	4	VLAN_MAP_0X4	See bit 3:0 of VLAN_PRI_MAP_REG0
15:12	R/W	3	VLAN_MAP_0X3	See bit 3:0 of VLAN_PRI_MAP_REG0

Bit	R/W	Inital Value	Mnemonic	Description
11:8	R/W	2	VLAN_MAP_0X2	See bit 3:0 of VLAN_PRI_MAP_REG0
7:4	R/W	1	VLAN_MAP_0X1	See bit 3:0 of VLAN_PRI_MAP_REG0
3:0	R/W	0	VLAN_MAP_0X0	3: DEI 2:0 PRIORITY

3.6.20 LOOP_CHECK_RESULT

Address 0x0654

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Table 3-126 summarizes the LOOP_CHECK_RESULT Register

Table 3-126. **LOOP CHECK RESULT Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:8	R/O	0	RESERVED	
7:4	R/O	0	PORT_NUM_NEW	When hardware checked loop occur, these bits indicate MAC address new port num.
3:0	R/O	0	PORT_NUM_OLD	When hardware checked loop occur, these bits indicate MAC address old port num.

3.6.21 PORT0_LOOKUP_CTRL

Address 0x0660

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Table 3-127 summarizes the PORT0_LOOKUP_CTRL Register

Table 3-127. **Port 0 Lookup Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_0	1'b1: Drop the multicast Packet from this port. Don't drop IGMP/MLD join/ leave and Special DIP packet.
30:29	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
28	R/W	0	UNI_LEAKY_EN_0	unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. if mac receive unicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base and 802.1q).
27	R/W	0	MULTI_LEAKY_EN_0	lso use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. if mac receive multicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_0 I	1'b1: if mac receive ARP frame from this port, it can cross all VLAN (include port base VLAN and 802.1q). 1'b0: ARP frame can't cross vlan Ingress port mirror. If this bit is set to 1'b1, all packets received from this port should be copied to mirror port.
25	R/W	0	NG_MIRROR_EN_0	Ingress port mirror. If this bit is set to 1'b1, all packets received from this port should be copied to mirror port.
24	R/O	0	RESERVED	
23	R/O	0	RESERVED	
22	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
21	R/W	1'b0	PORT_LOOPBACK_EN_0	1'b1: LOOP BACK. Packet sent in from this port will be sent out from the same port. This packet will not sent to other ports 1'b0: NORMAL FORWARDING
20	R/W	1'b1	LEARN_EN_0	Enable learn operation. 1'b1: enable hardware learn new MAC address into ARL table. 1'b0: won't learn new MAC address to ARL table
19	R/O	0	RESERVED	
18:16	R/W	3'h4	PORT_STATE_0	Port State. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree. 3'b000: Disable mode. The port is completely disable, and can't receive or transmit any frames. 3'b001: Blocking Mode. In this state, the port forwards received management frames to the designed port only. Any other frames can't be transmitted or received by the port, and without learning any SA address. 3'b010: Listening Mode. In this state, the port will receive and transmit only management frames, but without learning any SA address. Any other frames can't be transmitted or received by the port. 3'b011: Learning Mode. In this state, the port will learning all SA, and discard all frames except management frames, and only management frames allowed to be transmitted out. 3'b100: Forward Mode. In this state, the port will learning all SA, transmit and receive all frames like normal.
15	R/O	0	RESERVED	
14:12	R/O	0	RESERVED	
11	R/O	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_0	1'b1: force to use port base vlan enable. If this bit is set to 1'b1, use port base vlan & vlan table result to determine destination port.

Bit	R/W	Inital Value	Mnemonic	Description
9:8	R/W	2'b00	VLAN_MODE_0	802.1Q mode for this port. 2'b00: 802.1Q disable. Use port base VLAN only. 2'b01: fallback. Enable 802.1Q for all received frames. Don't discard ingress membership violation and use the port base VLAN if the frame's VID isn't contained in VLAN Table. 2'b10: check. Enable 802.1Q for all received frames. Don't discard ingress membership violation but discard frames which VID isn't contained in VLAN Table. 2'b11: secure. Enable 802.1Q for all received frames. Discard frames with ingress membership violation or whose VID isn't contained in the VLAN Table.
7	R/O	0	RESERVED	
6:0	R/W	'h7E	PORT_VID_MEM_0	Port Base VLAN Member. Each bit restrict which port can send frames to. To send frames to port0, bit 16 must be set to 1'b1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

3.6.22 PORT0_PRI_CTRL

Address 0x0664

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Table 3-128 summarizes the PORT0_PRI_CTRL Register

Table 3-128. **Port 0 Priority Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:21	R/O	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_0	
19	R/O	0	RESERVED	
18	R/W	0	DA_PRI_EN_0	1'b1: DA priority can be used for QOS.
17	R/W	0	VLAN_PRI_EN_0	1'b1: VLAN priority can be used for QOS.
16	R/W	0	IP_PRI_EN_0	1'b1: TOS/TC can be used for QOS.
15:8	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
7:6	R/W	0	DA_PRI_SEL_0	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_0	DA priority selected level for QOS.
3:2	R/W	2	IP_PRI_SEL_0	IP priority selected level for QOS.
1:0	R/O	0	RESERVED	

3.6.23 PORT0_LEARN_LIMIT

Address 0x0668

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Table 3-129 summarizes the PORT0_LEARN_LIMIT Register

Table 3-129. **Port 0 Learn Limit Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27	R/W	0	IGMP_LEARN_LIMIT_EN_0	1'b1: IGMP Learn Limit enable.
26	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_0	1'b1: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to IGMP_JOIN_CNT 1'b0: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to IGMP_JOIN_CNT_0
25:16	R/W	0	IGMP_JOIN_CNT_0	HARDWARE JOIN IGMP. WHEN JOIN NEW ENTRY OR NEW PORT TO IGMP +1, LEAVE OR AGE -1
15:12	R/W	7	SA_LEARN_STATUS_0	IF LESS THAN 0X7, DYNAMIC CAN BE FRESH TO SETTING VALUE AND AGE
11	R/W	0	SA_LEARN_LIMIT_EN_0	1'b1: SA Learn Limit enable.

Bit	R/W	Inital Value	Mnemonic	Description
10	R/W	0	SA_LEARN_LIMIT_DROP_EN_0	1'b1: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to SA_LEARN_CNT_0 1'b0: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to SA_LEARN_CNT_0
9:0	R/W	0	SA_LEARN_CNT_0	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: indicates no MAC limit number is 1 1: indicates the MAC limit number is 2 2: indicates the MAC limit number is 3 ... and so on ... until: 1023: indicates the MAC limit is 1024

3.6.24 PORT1_LOOKUP_CTRL

Address 0x066C

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Table 3-130 summarizes the PORT1_LOOKUP_CTRL Register

Table 3-130. **Port 1 Lookup Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_1	1'b1: Drop the multicast Packet from this port. Don't drop IGMP/MLD join/ leave and Special DIP packet.
30:29	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
28	R/W	0	UNI_LEAKY_EN_1	unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. if mac receive unicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base and 802.1q).
27	R/W	0	MULTI_LEAKY_EN_1	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. if mac receive multicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_1	1'b1: if mac receive ARP frame from this port, it can cross all VLAN (include port base VLAN and 802.1q). 1'b0: ARP frame can't cross vlan
25	R/W	0	ING_MIRROR_EN_1	Ingress port mirror. If this bit is set to 1'b1, all packets received from this port should be copied to mirror port.
24	R/O	0	RESERVED	
23	R/O	0	RESERVED	
22	R/O	0	RESERVED	
21	R/W	1'b0	PORT_LOOPBACK_EN_1	1'b1: LOOP BACK. Packet sent in from this port will be sent out from the same port. This packet will not sent to other ports 1'b0: NORMAL FORWARDING

Bit	R/W	Inital Value	Mnemonic	Description
20	R/W	1'b1	LEARN_EN_1	Enable learn operation. 1'b1: enable hardware learn new MAC address into ARL table. 1'b0: won't learn new MAC address to ARL table
19	R/O	0	RESERVED	
18:16	R/W	3'h4	PORT_STATE_1	Port State. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree. 3'b000: Disable mode. The port is completely disable, and can't receive or transmit any frames. 3'b001: Blocking Mode. In this state, the port forwards received management frames to the designed port only. Any other frames can't be transmitted or received by the port, and without learning any SA address. 3'b010: Listening Mode. In this state, the port will receive and transmit only management frames, but without learning any SA address. Any other frames can't be transmitted or received by the port. 3'b011: Learning Mode. In this state, the port will learning all SA, and discard all frames except management frames, and only management frames allowed to be transmitted out. 3'b100: Forward Mode. In this state, the port will learning all SA, transmit and receive all frames like normal.
15	R/O	0	RESERVED	
14:12	R/O	0	RESERVED	
11	R/O	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_1	1'b1: force to use port base vlan enable. If this bit is set to 1'b1, use port base vlan & vlan table result to determine destination port.

Bit	R/W	Inital Value	Mnemonic	Description
9:8	R/W	2'b00	VLAN_MODE_1	802.1Q mode for this port. 2'b00: 802.1Q disable. Use port base VLAN only. 2'b01: fallback. Enable 802.1Q for all received frames. Don't discard ingress membership violation and use the port base VLAN if the frame's VID isn't contained in VLAN Table. 2'b10: check. Enable 802.1Q for all received frames. Don't discard ingress membership violation but discard frames which VID isn't contained in VLAN Table. 2'b11: secure. Enable 802.1Q for all received frames. Discard frames with ingress membership violation or whose VID isn't contained in the VLAN Table.
7	R/O	0	RESERVED	
6:0	R/W	'h7D	PORT_VID_MEM_1	Port Base VLAN Member. Each bit restrict which port can send frames to. To send frames to port0, bit 16 must be set to 1'b1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

3.6.25 PORT1_PRI_CTRL *Address 0x0670*

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Table 3-131, "Port 1 Priority Control Register," on page 147 Port 1 Priority Control Register

Table 3-131. **Port 1 Priority Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:21	R/O	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_1	
19	R/O	0	RESERVED	
18	R/W	0	DA_PRI_EN_1	1'b1: DA priority can be used for QOS.
17	R/W	0	VLAN_PRI_EN_1	1'b1: VLAN priority can be used for QOS.
16	R/W	0	IP_PRI_EN_1	1'b1: TOS/TC can be used for QOS.
15:8	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
7:6	R/W	0	DA_PRI_SEL_1	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_1	
3:2	R/W	2	IP_PRI_SEL_1	DA priority selected level for QOS.
1:0	R/O	0	RESERVED	IP priority selected level for QOS.

3.6.26 PORT1_LEARN_LIMIT

Address 0x0674

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Table 3-132, "Port 1 Learn Limit Register," on page 148 summarizes the PORT1_LEARN_LIMIT Register

Table 3-132. **Port 1 Learn Limit Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27	R/W	0	IGMP_LEARN_LIMIT_EN_1	1'b1: IGMP Learn Limit enable.
26	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_1	1'b1: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to IGMP_JOIN_CNT_1 1'b0: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to IGMP_JOIN_CNT_1
25:16	R/W	0	IGMP_JOIN_CNT_1	HARDWARE JOIN IGMP. WHEN JOIN NEW ENTRY OR NEW PORT TO IGMP +1, LEAVE OR AGE -1
15:12	R/W	7	SA_LEARN_STATUS_1	IF LESS THAN 0X7, DYNAMIC CAN BE FRESH TO SETTING VALUE AND AGE
11	R/W	0	SA_LEARN_LIMIT_EN_1	1'b1: SA Learn Limit enable.

Bit	R/W	Inital Value	Mnemonic	Description
10	R/W	0	SA_LEARN_LIMIT_DROP_EN_1	1'b1: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to SA_LEARN_CNT_1 1'b0: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to SA_LEARN_CNT_1
9:0	R/W	0	SA_LEARN_CNT_1	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: indicates no MAC limit number is 1 1: indicates the MAC limit number is 2 2: indicates the MAC limit number is 3 ... and so on ... until: 1023: indicates the MAC limit is 1024

3.6.27 PORT2_LOOKUP_CTRL

Address 0x0678

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Table 3-133 summarizes the PORT2_LOOKUP_CTRL Register

Table 3-133. **Port 2 Lookup Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_2	1'b1: Drop the multicast Packet from this port. Don't drop IGMP/MLD join/ leave and Special DIP packet.
30:29	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
28	R/W	0	UNI_LEAKY_EN_2	unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. if mac receive unicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base and 802.1q).
27	R/W	0	MULTI_LEAKY_EN_2	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. if mac receive multicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_2	1'b1: if mac receive ARP frame from this port, it can cross all VLAN (include port base VLAN and 802.1q). 1'b0: ARP frame can't cross vlan
25	R/W	0	ING_MIRROR_EN_2	Ingress port mirror. If this bit is set to 1'b1, all packets received from this port should be copied to mirror port.
24	R/O	0	RESERVED	
23	R/O	0	RESERVED	
22	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
21	R/W	1'b0	PORT_LOOPBACK_EN_2	1'b1: LOOP BACK. Packet sent in from this port will be sent out from the same port. This packet will not sent to other ports 1'b0: NORMAL FORWARDING Enable learn operation. 1'b1: enable hardware learn new MAC address into ARL table. 1'b0: won't learn new MAC address to ARL table
20	R/W	1'b1	LEARN_EN_2	
19	R/O	0	RESERVED	
18:16	R/W	3'h4	PORT_STATE_2	
15	R/O	0	RESERVED	
14:12	R/O	0	RESERVED	
11	R/O	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_2	
9:8	R/W	2'b00	VLAN_MODE_2	802.1Q mode for this port. 2'b00: 802.1Q disable. Use port base VLAN only. 2'b01: fallback. Enable 802.1Q for all received frames. Don't discard ingress membership violation and use the port base VLAN if the frame's VID isn't contained in VLAN Table. 2'b10: check. Enable 802.1Q for all received frames. Don't discard ingress membership violation but discard frames which VID isn't contained in VLAN Table. 2'b11: secure. Enable 802.1Q for all received frames. Discard frames with ingress membership violation or whose VID isn't contained in the VLAN Table.
7	R/W	0'	RESERVED	
6:0	R/W	h7B	PORT_VID_MEM_2	Port Base VLAN Member. Each bit restrict which port can send frames to. To send frames to port0, bit 16 must be set to 1'b1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

3.6.28 PORT2_PRI_CTRL

Address 0x067C

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Table 3-134 summarizes the PORT2_PRI_CTRL Register

Table 3-134. **Port 2 Priority Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:21	R/O	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_2	
19	R/O	0	RESERVED	
18	R/W	0	DA_PRI_EN_2	1'b1: DA priority can be used for QOS.
17	R/W	0	VLAN_PRI_EN_2	1'b1: VLAN priority can be used for QOS.
16	R/W	0	IP_PRI_EN_2	1'b1: TOS/TC can be used for QOS.
15:8	R/O	0	RESERVED	
7:6	R/W	0	DA_PRI_SEL_2	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_2	DA priority selected level for QOS.
3:2	R/W	2	IP_PRI_SEL_2	IP priority selected level for QOS.
1:0	R/O	0	RESERVED	

3.6.29 PORT2_LEARN_LIMIT

Address 0x0680

SFT&HW RST

Table 3-135 summarizes the PORT2_LEARN_LIMIT Register

Table 3-135. **Port 2 Learn Limit Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27	R/W	0	IGMP_LEARN_LIMIT_EN_2	1'b1: IGMP Learn Limit enable.

Bit	R/W	Inital Value	Mnemonic	Description
26	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_2	1'b1: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to IGMP_JOIN_CNT_2 1'b0: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to IGMP_JOIN_CNT_2
25:16	R/W	0	IGMP_JOIN_CNT_2	HARDWARE JOIN IGMP. WHEN JOIN NEW ENTRY OR NEW PORT TO IGMP +1, LEAVE OR AGE -1
15:12	R/W	7	SA_LEARN_STATUS_2	IF LESS THAN 0X7, DYNAMIC CAN BE FRESH TO SETTING VALUE AND AGE
11	R/W	0	SA_LEARN_LIMIT_EN_2	1'b1: SA Learn Limit enable.
10	R/W	0	SA_LEARN_LIMIT_DROP_EN_2	1'b1: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to SA_LEARN_CNT_2 1'b0: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to SA_LEARN_CNT_2
9:0	R/W	0	SA_LEARN_CNT_2	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: indicates no MAC limit number is 1 1: indicates the MAC limit number is 2 2: indicates the MAC limit number is 3 ... and so on ... until: 1023: indicates the MAC limit is 1024

3.6.30 PORT3_LOOKUP_CTRL

Address 0x0684

SFT&HW RST

Table 3-136 summarizes the PORT3_LOOKUP_CTRL Register

Table 3-136. **Port 3 Lookup Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_3	1'b1: Drop the multicast Packet from this port. Don't drop IGMP/MLD join/ leave and Special DIP packet.
30:29	R/O	0	RESERVED	
28	R/W	0	UNI_LEAKY_EN_3	unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. if mac receive unicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base and 802.1q).
27	R/W	0	MULTI_LEAKY_EN_3	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. if mac receive multicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_3	1'b1: if mac receive ARP frame from this port, it can cross all VLAN (include port base VLAN and 802.1q). 1'b0: ARP frame can't cross vlan
25	R/W	0	ING_MIRROR_EN_3	Ingress port mirror. If this bit is set to 1'b1, all packets received from this port should be copied to mirror port.
24	R/O	0	RESERVED	
23	R/O	0	RESERVED	
22	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
21	R/W	1'b0	PORT_LOOPBACK_EN_3	1'b1: LOOP BACK. Packet sent in from this port will be sent out from the same port. This packet will not sent to other ports 1'b0: NORMAL FORWARDING
20	R/W	1'b1	LEARN_EN_3	Enable learn operation. 1'b1: enable hardware learn new MAC address into ARL table. 1'b0: won't learn new MAC address to ARL table
19	R/O	0	RESERVED	
18:16	R/W	3'h4	PORT_STATE_3	Port State. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree. 3'b000: Disable mode. The port is completely disable, and can't receive or transmit any frames. 3'b001: Blocking Mode. In this state, the port forwards received management frames to the designed port only. Any other frames can't be transmitted or received by the port, and without learning any SA address. 3'b010: Listening Mode. In this state, the port will receive and transmit only management frames, but without learning any SA address. Any other frames can't be transmitted or received by the port. 3'b011: Learning Mode. In this state, the port will learning all SA, and discard all frames except management frames, and only management frames allowed to be transmitted out. 3'b100: Forward Mode. In this state, the port will learning all SA, transmit and receive all frames like normal.
15	R/O	0	RESERVED	
14:12	R/O	0	RESERVED	
11	R/O	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_3	1'b1: force to use port base vlan enable. If this bit is set to 1'b1, use port base vlan & vlan table result to determine destination port.

Bit	R/W	Inital Value	Mnemonic	Description
9:8	R/W	2'b00	VLAN_MODE_3	802.1Q mode for this port. 2'b00: 802.1Q disable. Use port base VLAN only. 2'b01: fallback. Enable 802.1Q for all received frames. Don't discard ingress membership violation and use the port base VLAN if the frame's VID isn't contained in VLAN Table. 2'b10: check. Enable 802.1Q for all received frames. Don't discard ingress membership violation but discard frames which VID isn't contained in VLAN Table. 2'b11: secure. Enable 802.1Q for all received frames. Discard frames with ingress membership violation or whose VID isn't contained in the VLAN Table.
7	R/W	0'	RESERVED	
6:0	R/W	h7B	PORT_VID_MEM_3	Port Base VLAN Member. Each bit restrict which port can send frames to. To send frames to port0, bit 16 must be set to 1'b1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

3.6.31 PORT3_PRI_CTRL

Address 0x0688

SFT&HW RST

Table 3-137 summarizes the PORT3_PRI_CTRL Register

Table 3-137. **Port 3 Priority Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:21	R/O	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_3	
19	R/O	0	RESERVED	
18	R/W	0	DA_PRI_EN_3	1'b1: DA priority can be used for QOS.
17	R/W	0	VLAN_PRI_EN_3	1'b1: VLAN priority can be used for QOS.
16	R/W	0	IP_PRI_EN_3	1'b1: TOS/TC can be used for QOS.
15:8	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
7:6	R/W	0	DA_PRI_SEL_3	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_3	DA priority selected level for QOS.
3:2	R/W	2	IP_PRI_SEL_3	IP priority selected level for QOS.
1:0	R/O	0	RESERVED	

3.6.32 PORT3_LEARN_LIMIT

Address 0x068C

SFT&HW RST

Table 3-138 Port 3 Learn Limit Control Register

Table 3-138. **Port 3 Learn Limit Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27	R/W	0	IGMP_LEARN_LIMIT_EN_3	1'b1: IGMP Learn Limit enable.
26	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_3	1'b1: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to IGMP_JOIN_CNT_3 1'b0: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to IGMP_JOIN_CNT_3
25:16	R/W	0	IGMP_JOIN_CNT_3	HARDWARE JOIN IGMP. WHEN JOIN NEW ENTRY OR NEW PORT TO IGMP +1, LEAVE OR AGE -1
15:12	R/W	7	SA_LEARN_STATUS_3	IF LESS THAN 0X7, DYNAMIC CAN BE FRESH TO SETTING VALUE AND AGE
11	R/W	0	SA_LEARN_LIMIT_EN_3	1'b1: SA Learn Limit enable.

Bit	R/W	Inital Value	Mnemonic	Description
10	R/W	0	SA_LEARN_LIMIT_DROP_EN_3	1'b1: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to SA_LEARN_CNT_3 1'b0: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to SA_LEARN_CNT_3
9:0	R/W	0	SA_LEARN_CNT_3	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: indicates no MAC limit number is 1 1: indicates the MAC limit number is 2 2: indicates the MAC limit number is 3 ... and so on ... until: 1023: indicates the MAC limit is 1024

3.6.33 PORT4_LOOKUP_CTRL

Address 0x0690

SFT&HW RST

Table 3-139 summarizes the PORT4_LOOKUP_CTRL Register

Table 3-139. **Port 4 Lookup Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_4	1'b1: Drop the multicast Packet from this port. Don't drop IGMP/MLD join/leave and Special DIP packet.
30:29	R/O	0	RESERVED	
28	R/W	0	UNI_LEAKY_EN_4	unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. if mac receive unicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base and 802.1q).

Bit	R/W	Inital Value	Mnemonic	Description
27	R/W	0	MULTI_LEAKY_EN_4	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. if mac receive multicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_4	1'b1: if mac receive ARP frame from this port, it can cross all VLAN (include port base VLAN and 802.1q). 1'b0: ARP frame can't cross vlan
25	R/W	0	ING_MIRROR_EN_4	Ingress port mirror. If this bit is set to 1'b1, all packets received from this port should be copied to mirror port.
24	R/O	0	RESERVED	
23	R/O	0	RESERVED	
22	R/O	0	RESERVED	
21	R/W	1'b0	PORT_LOOPBACK_EN_4	1'b1: LOOP BACK. Packet sent in from this port will be sent out from the same port. This packet will not sent to other ports 1'b0: NORMAL FORWARDING
20	R/W	1'b1	LEARN_EN_4	Enable learn operation. 1'b1: enable hardware learn new MAC address into ARL table. 1'b0: won't learn new MAC address to ARL table
19	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
18:16	R/O	3'h4	PORT_STATE_4	Port State. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree. 3'b000: Disable mode. The port is completely disable, and can't receive or transmit any frames. 3'b001: Blocking Mode. In this state, the port forwards received management frames to the designed port only. Any other frames can't be transmitted or received by the port, and without learning any SA address. 3'b010: Listening Mode. In this state, the port will receive and transmit only management frames, but without learning any SA address. Any other frames can't be transmitted or received by the port. 3'b011: Learning Mode. In this state, the port will learning all SA, and discard all frames except management frames, and only management frames allowed to be transmitted out. 3'b100: Forward Mode. In this state, the port will learning all SA, transmit and receive all frames like normal.
15	R/O	0	RESERVED	
14:12	R/O	0	RESERVED	
11	R/W	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_4	1'b1: force to use port base vlan enable. If this bit is set to 1'b1, use port base vlan & vlan table result to determine destination port.
9:8	R/W	2'0	VLAN_MODE_4	802.1Q mode for this port. 2'b00: 802.1Q disable. Use port base VLAN only. 2'b01: fallback. Enable 802.1Q for all received frames. Don't discard ingress membership violation and use the port base VLAN if the frame's VID isn't contained in VLAN Table. 2'b10: check. Enable 802.1Q for all received frames. Don't discard ingress membership violation but discard frames which VID isn't contained in VLAN Table. 2'b11: secure. Enable 802.1Q for all received frames. Discard frames with ingress membership violation or whose VID isn't contained in the VLAN Table.
7	R/O	'h6F	RESERVED	
6:0	R/W	b00	PORT_VID_MEM_4	Port Base VLAN Member. Each bit restrict which port can send frames to. To send frames to port0, bit 16 must be set to 1'b1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

3.6.34 PORT4_PRI_CTRL Address 0x0694

SFT&HW RST

Table 3-140 summarizes the PORT4_PRI_CTRL Register

Table 3-140. **Port 4 Priority Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:21	R/O	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_4	1'b1: DA priority can be used for QOS. 1'b1: VLAN priority can be used for QOS. 1'b1: TOS/TC can be used for QOS.
19	R/O	0	RESERVED	
18	R/W	0	DA_PRI_EN_4	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
17	R/W	0	VLAN_PRI_EN_4	DA priority selected level for QOS.
16	R/W	0	IP_PRI_EN_4	IP priority selected level for QOS.
15:8	R/O	0	RESERVED	
7:6	R/W	0	DA_PRI_SEL_4	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_4	DA priority selected level for QOS.
3:2	R/W	2	IP_PRI_SEL_4	IP priority selected level for QOS.
1:0	R/O	0	RESERVED	

3.6.35 PORT4_LEARN_LIMIT

Address 0x0698

SFT&HW RST

Table 3-141 summarizes the PORT4_LEARN_LIMIT Register

Table 3-141. **Port 4 Learn Limit Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27	R/W	0	IGMP_LEARN_LIMIT_EN_4	1'b1: IGMP Learn Limit enable.
26	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_4	1'b1: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to IGMP_JOIN_CNT_4 1'b0: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to IGMP_JOIN_CNT_4
25:16	R/W	0	IGMP_JOIN_CNT_4	Hardware join IGMP. When joiing new entry or new port to IGMP +1, leave or AGE -1.
15:12	R/W	7	SA_LEARN_STATUS_4	If less than 0x7, dynamic can be refreshed to setting value and age
11	R/W	0	SA_LEARN_LIMIT_EN_4	1'b1: SA Learn Limit enable.
10	R/W	0	SA_LEARN_LIMIT_DROP_EN_4	1'b1: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to SA_LEARN_CNT_4 1'b0: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to SA_LEARN_CNT_4
9:0	R/W	0	SA_LEARN_CNT_4	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: indicates no MAC limit number is 1 1: indicates the MAC limit number is 2 2: indicates the MAC limit number is 3 ... and so on ... until: 1023: indicates the MAC limit is 1024

3.6.36 PORT5_LOOKUP_CTRL

Address 0x069C

SFT&HW RST

Table 3-142 summarizes the PORT5_LOOKUP_CTRL Register

Table 3-142. **Port 5 Lookup Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_5	1'b1: Drop the multicast Packet from this port. Don't drop IGMP/MLD join/leave and Special DIP packet.
30:29	R/O	0	RESERVED	
28	R/W	0	UNI_LEAKY_EN_5	unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. if mac receive unicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base and 802.1q).
27	R/W	0	MULTI_LEAKY_EN_5	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. if mac receive multicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_5	1'b1: if mac receive ARP frame from this port, it can cross all VLAN (include port base VLAN and 802.1q). 1'b0: ARP frame can't cross vlan
25	R/W	0	ING_MIRROR_EN_5	Ingress port mirror. If this bit is set to 1'b1, all packets received from this port should be copied to mirror port.
24	R/O	0	RESERVED	
23	R/O	0	RESERVED	
22	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
21	R/W	1'b0	PORT_LOOPBACK_EN_5	1'b1: LOOP BACK. Packet sent in from this port will be sent out from the same port. This packet will not sent to other ports 1'b0: NORMAL FORWARDING
20	R/W	1'b1	LEARN_EN_5	Enable learn operation. 1'b1: enable hardware learn new MAC address into ARL table. 1'b0: won't learn new MAC address to ARL table
19	R/O	0	RESERVED	
18:16	R/O	3'h4	PORT_STATE_5	Port State. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree. 3'b000: Disable mode. The port is completely disable, and can't receive or transmit any frames. 3'b001: Blocking Mode. In this state, the port forwards received management frames to the designed port only. Any other frames can't be transmitted or received by the port, and without learning any SA address. 3'b010: Listening Mode. In this state, the port will receive and transmit only management frames, but without learning any SA address. Any other frames can't be transmitted or received by the port. 3'b011: Learning Mode. In this state, the port will learning all SA, and discard all frames except management frames, and only management frames allowed to be transmitted out. 3'b100: Forward Mode. In this state, the port will learning all SA, transmit and receive all frames like normal.
15	R/O	0	RESERVED	
14:12	R/O	0	RESERVED	
11	R/W	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_5	1'b1: force to use port base vlan enable. If this bit is set to 1'b1, use port base vlan & vlan table result to determine destination port.
9:8	R/W	2'0	VLAN_MODE_5	802.1Q mode for this port. 2'b00: 802.1Q disable. Use port base VLAN only. 2'b01: fallback. Enable 802.1Q for all received frames. Don't discard ingress membership violation and use the port base VLAN if the frame's VID isn't contained in VLAN Table. 2'b10: check. Enable 802.1Q for all received frames. Don't discard ingress membership violation but discard frames which VID isn't contained in VLAN Table. 2'b11: secure. Enable 802.1Q for all received frames. Discard frames with ingress membership violation or whose VID isn't contained in the VLAN Table.

Bit	R/W	Inital Value	Mnemonic	Description
7	R/O	'h6F	RESERVED	
6:0	R/W	b00	PORT_VID_MEM_5	Port Base VLAN Member. Each bit restrict which port can send frames to. To send frames to port0, bit 16 must be set to 1'b1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

3.6.37 PORT5_PRI_CTRL

Address 0x06A0

SFT&HW RST

Table 3-143 summarizes the PORT5_PRI_CTRL Register

Table 3-143. **Port 5 Priority Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:21	R/O	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_5	1'b1: DA priority can be used for QOS. 1'b1: VLAN priority can be used for QOS. 1'b1: TOS/TC can be used for QOS.
19	R/O	0	RESERVED	
18	R/W	0	DA_PRI_EN_5	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
17	R/W	0	VLAN_PRI_EN_5	DA priority selected level for QOS.
16	R/W	0	IP_PRI_EN_5	IP priority selected level for QOS.
15:8	R/O	0	RESERVED	
7:6	R/W	0	DA_PRI_SEL_5	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_5	DA priority selected level for QOS.

Bit	R/W	Inital Value	Mnemonic	Description
3:2	R/W	2	IP_PRI_SEL_5	IP priority selected level for QOS.
1:0	R/O	0	RESERVED	

3.6.38 PORT5_LEARN_LIMIT

Address 0x06A4

SFT&HW RST

Table 3-144 summarizes the PORT5_LEARN_LIMIT Register

Table 3-144. **Port 5 Learn Limit Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27	R/W	0	IGMP_LEARN_LIMIT_EN_5	1'b1: IGMP Learn Limit enable.
26	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_5	1'b1: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to IGMP_JOIN_CNT_4 1'b0: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to IGMP_JOIN_CNT_4
25:16	R/W	0	IGMP_JOIN_CNT_5	HARDWARE JOIN IGMP. WHEN JOIN NEW ENTRY OR NEW PORT TO IGMP +1, LEAVE OR AGE -1
15:12	R/W	7	SA_LEARN_STATUS_5	IF LESS THAN 0X7, DYNAMIC CAN BE FRESH TO SETTING VALUE AND AGE
11	R/W	0	SA_LEARN_LIMIT_EN_5	1'b1: SA Learn Limit enable.

Bit	R/W	Inital Value	Mnemonic	Description
10	R/W	0	SA_LEARN_LIMIT_DROP_EN_5	1'b1: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to SA_LEARN_CNT_4 1'b0: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to SA_LEARN_CNT_4
9:0	R/W	0	SA_LEARN_CNT_5	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: indicates no MAC limit number is 1 1: indicates the MAC limit number is 2 2: indicates the MAC limit number is 3 ... and so on ... until: 1023: indicates the MAC limit is 1024

3.6.39 PORT6_LOOKUP_CTRL

Address 0x06A8

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page 167 summarizes the PORT6_LOOKUP_CTRL Register

Table 3-145. **Port 6 Lookup Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_6	1'b1: Drop the multicast Packet from this port. Don't drop IGMP/MLD join/ leave and Special DIP packet.
30:29	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
28	R/W	0	UNI_LEAKY_EN_6	unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. if mac receive unicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base and 802.1q).
27	R/W	0	MULTI_LEAKY_EN_6	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. if mac receive multicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_6	1'b1: if mac receive ARP frame from this port, it can cross all VLAN (include port base VLAN and 802.1q). 1'b0: ARP frame can't cross vlan
25	R/W	0	ING_MIRROR_EN_6	Ingress port mirror. If this bit is set to 1'b1, all packets received from this port should be copied to mirror port.
24	R/O	0	RESERVED	
23	R/O	0	RESERVED	
22	R/O	0	RESERVED	
21	R/W	1'b0	PORT_LOOPBACK_EN_6	1'b1: LOOP BACK. Packet sent in from this port will be sent out from the same port. This packet will not sent to other ports 1'b0: NORMAL FORWARDING

Bit	R/W	Inital Value	Mnemonic	Description
20	R/W	1'b1	LEARN_EN_6	Enable learn operation. 1'b1: enable hardware learn new MAC address into ARL table. 1'b0: won't learn new MAC address to ARL table
19	R/O	0	RESERVED	
18:16	R/O	3'h4	PORT_STATE_6	Port State. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree. 3'b000: Disable mode. The port is completely disable, and can't receive or transmit any frames. 3'b001: Blocking Mode. In this state, the port forwards received management frames to the designed port only. Any other frames can't be transmitted or received by the port, and without learning any SA address. 3'b010: Listening Mode. In this state, the port will receive and transmit only management frames, but without learning any SA address. Any other frames can't be transmitted or received by the port. 3'b011: Learning Mode. In this state, the port will learning all SA, and discard all frames except management frames, and only management frames allowed to be transmitted out. 3'b100: Forward Mode. In this state, the port will learning all SA, transmit and receive all frames like normal.
15	R/O	0	RESERVED	
14:12	R/O	0	RESERVED	
11	R/W	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_6	1'b1: force to use port base vlan enable. If this bit is set to 1'b1, use port base vlan & vlan table result to determine destination port.

Bit	R/W	Inital Value	Mnemonic	Description
9:8	R/W	2'0	VLAN_MODE_6	802.1Q mode for this port. 2'b00: 802.1Q disable. Use port base VLAN only. 2'b01: fallback. Enable 802.1Q for all received frames. Don't discard ingress membership violation and use the port base VLAN if the frame's VID isn't contained in VLAN Table. 2'b10: check. Enable 802.1Q for all received frames. Don't discard ingress membership violation but discard frames which VID isn't contained in VLAN Table. 2'b11: secure. Enable 802.1Q for all received frames. Discard frames with ingress membership violation or whose VID isn't contained in the VLAN Table.
7	R/O	'h6F	RESERVED	
6:0	R/W	b00	PORT_VID_MEM_6	Port Base VLAN Member. Each bit restrict which port can send frames to. To send frames to port0, bit 16 must be set to 1'b1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

3.6.40 PORT6_PRI_CTRL

Address 0x06AC

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Table 3-146 summarizes the PORT6_PRI_CTRL Register

Table 3-146. **Port 6 Priority Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:21	R/O	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_6	1'b1: DA priority can be used for QOS. 1'b1: VLAN priority can be used for QOS. 1'b1: TOS/TC can be used for QOS.
19	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
18	R/W	0	DA_PRI_EN_6	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
17	R/W	0	VLAN_PRI_EN_6	DA priority selected level for QOS.
16	R/W	0	IP_PRI_EN_6	IP priority selected level for QOS.
15:8	R/O	0	RESERVED	
7:6	R/W	0	DA_PRI_SEL_6	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_6	DA priority selected level for QOS.
3:2	R/W	2	IP_PRI_SEL_6	IP priority selected level for QOS.
1:0	R/O	0	RESERVED	

3.6.41 PORT6_LEARN_LIMIT

Address 0x06B0

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Table 3-147 summarizes the PORT6_LEARN_LIMIT Register

Table 3-147. **Port 6 Learn Limit Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	RESERVED	
27	R/W	0	IGMP_LEARN_LIMIT_EN_6	1'b1: IGMP Learn Limit enable.

Bit	R/W	Inital Value	Mnemonic	Description
26	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_6	1'b1: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to IGMP_JOIN_CNT_4 1'b0: if IGMP GROUP ADDR is not in ARL table or IGMP GROUP ADDR in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to IGMP_JOIN_CNT_4
25:16	R/W	0	IGMP_JOIN_CNT_6	HARDWARE JOIN IGMP. WHEN JOIN NEW ENTRY OR NEW PORT TO IGMP +1, LEAVE OR AGE -1
15:12	R/W	7	SA_LEARN_STATUS_6	IF LESS THAN 0X7, DYNAMIC CAN BE FRESH TO SETTING VALUE AND AGE
11	R/W	0	SA_LEARN_LIMIT_EN_6	1'b1: SA Learn Limit enable.
10	R/W	0	SA_LEARN_LIMIT_DROP_EN_6	1'b1: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be dropped when Learned MAC address counter is equal to SA_LEARN_CNT_4 1'b0: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be redirect to cpu when Learned MAC address counter is equal to SA_LEARN_CNT_4
9:0	R/W	0	SA_LEARN_CNT_6	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: indicates no MAC limit number is 1 1: indicates the MAC limit number is 2 2: indicates the MAC limit number is 3 ... and so on ... until: 1023: indicates the MAC limit is 1024

3.6.42 GOL_TRUNK_CTRL0

Address 0x0700

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Table 3-148 summarizes the GOL_TRUNK_CTRL0 Register 0

Table 3-148. **Global Trunk Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	TRUNK3_EN	TRUNK 3 Enable
30:24	R/W	0	TRUNK3_MEM	TRUNK 3 member bitmap
23	R/W	0	TRUNK2_EN	TRUNK 2 Enable
22:16	R/W	0	TRUNK2_MEM	TRUNK 2 member bitmap
15	R/W	0	TRUNK1_EN	TRUNK 1 Enable
14:8	R/W	0	TRUNK1_MEM	TRUNK 1 member bitmap
7	R/W	0	TRUNK0_EN	TRUNK 0 Enable
6:0	R/W	0	TRUNK0_MEM	TRUNK 0 member bitmap

3.6.43 GOL_TRUNK_CTRL1

Address 0x0704

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Table 3-149 summarizes the GOL_TRUNK_CTRL1 Register 1

Table 3-149. **Global Trunk Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	TRUNK1_MEM3_EN	ENABLE TRUNK 1 member 3
30:28	R/W	0	TRUNK1_MEM3_NUM	TRUNK 1 member 3 port number
27	R/W	0	TRUNK1_MEM2_EN	ENABLE TRUNK 1 member 2
26:24	R/W	0	TRUNK1_MEM2_NUM	TRUNK 1 member 2 port number
23	R/W	0	TRUNK1_MEM1_EN	ENABLE TRUNK 1 member 1
22:20	R/W	0	TRUNK1_MEM1_NUM	TRUNK 1 member 1 port number
19	R/W	0	TRUNK1_MEM0_EN	ENABLE TRUNK 1 member 0
18:16	R/W	0	TRUNK1_MEM0_NUM	TRUNK 1 member 0 port number
15	R/W	0	TRUNK0_MEM3_EN	ENABLE TRUNK 0 member 3

Bit	R/W	Inital Value	Mnemonic	Description
14:12	R/W	0	TRUNK0_MEM3_NUM	TRUNK 0 member 3 port number
11	R/W	0	TRUNK0_MEM2_EN	ENABLE TRUNK 0 member 2
10:8	R/W	0	TRUNK0_MEM2_NUM	TRUNK 0 member 2 port number
7	R/W	0	TRUNK0_MEM1_EN	ENABLE TRUNK 0 member 1
6:4	R/W	0	TRUNK0_MEM1_NUM	TRUNK 0 member 1 port number
3	R/W	0	TRUNK0_MEM0_EN	ENABLE
2:0	R/W	0	TRUNK0_MEM0_NUM	TRUNK 0 member0 port number

3.6.44 GOL_TRUNK_CTRL2

Address 0x0708

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Table 3-150, "Global Trunk Control Register 2," on page 174 summarizes the GOL_TRUNK_CTRL2 Register 2

Table 3-150. **Global Trunk Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	TRUNK3_MEM3_EN	ENABLE TRUNK 3 member 3
30:28	R/W	0	TRUNK3_MEM3_NUM	TRUNK 3 member 3 port number
27	R/W	0	TRUNK3_MEM2_EN	ENABLE TRUNK 3 member 2
26:24	R/W	0	TRUNK3_MEM2_NUM	TRUNK 3 member 2 port number
23	R/W	0	TRUNK3_MEM1_EN	ENABLE TRUNK 3 member 1
22:20	R/W	0	TRUNK3_MEM1_NUM	TRUNK 3 member 1 port number
19	R/W	0	TRUNK3_MEM0_EN	ENABLE TRUNK 3 member 0

Bit	R/W	Inital Value	Mnemonic	Description
18:16	R/W	0	TRUNK3_MEM0_NUM	TRUNK 3 member0 port number
15	R/W	0	TRUNK2_MEM3_EN	ENABLE TRUNK 2 member 3
14:12	R/W	0	TRUNK2_MEM3_NUM	TRUNK 2 member 3 port number
11	R/W	0	TRUNK2_MEM2_EN	ENABLE TRUNK 2 member 2
10:8	R/W	0	TRUNK2_MEM2_NUM	TRUNK 2 member 2 port number
7	R/W	0	TRUNK2_MEM1_EN	ENABLE TRUNK 2 member 1
6:4	R/W	0	TRUNK2_MEM1_NUM	TRUNK 2 member 1 port number
3	R/W	0	TRUNK2_MEM0_EN	ENABLE TRUNK 2 member 0
2:0	R/W	0	TRUNK2_MEM0_NUM	TRUNK 2 member0 port number

3.7 QM REGISTER(BASE ADDR:0x0800)

Table 3-151, "Parser Register Summary," on page 175 summarizes the Lookup registers.

Table 3-151. **Parser Register Summary**

Name	Address	Reset
GLOBAL FLOW CTRL THESHOLD REGISTER	0x0800	HARD & SOFT
QM CONTROL REGISTER	0x0808	HARD & SOFT
WAN PRI TO QUEUE MAPPING REGISTER	0x0810	HARD & SOFT
LAN PRI TO QUEUE MAPPING REGISTER	0x0814	HARD & SOFT
PORT0 WRR CONTROL REGISTER	0x0830	HARD & SOFT
PORT1 WRR CONTROL REGISTER	0x0834	HARD & SOFT
PORT2 WRR CONTROL REGISTER	0x0838	HARD & SOFT

Table 3-151. **Parser Register Summary (continued)**

Name	Address	Reset
PORT3 WRR CONTROL REGISTER	0x083C	HARD & SOFT
PORT4 WRR CONTROL REGISTER	0x0840	HARD & SOFT
PORT5 WRR CONTROL REGISTER	0x0844	HARD & SOFT
PORT6 WRR CONTROL REGISTER	0x0848	HARD & SOFT
PORT0 EGRESS RATE LIMIT CONTROL REGISTER	0x0890~0x08AC	HARD & SOFT
PORT1 EGRESS RATE LIMIT CONTROL REGISTER	0x08B0~0x08CC	HARD & SOFT
PORT2 EGRESS RATE LIMIT CONTROL REGISTER	0x08D0~0x08EC	HARD & SOFT
PORT3 EGRESS RATE LIMIT CONTROL REGISTER	0x08F0~0x090C	HARD & SOFT
PORT4 EGRESS RATE LIMIT CONTROL REGISTER	0x0910~0x092C	HARD & SOFT
PORT5 EGRESS RATE LIMIT CONTROL REGISTER	0x0930~0x094C	HARD & SOFT
PORT6 EGRESS RATE LIMIT CONTROL REGISTER	0x0950~0x096C	HARD & SOFT
PORT0 HOL CONTROL REGISTER	0x0970~0x0974	HARD & SOFT
PORT1 HOL CONTROL REGISTER	0x0978~0x097C	HARD & SOFT
PORT2 HOL CONTROL REGISTER	0x0980~0x0984	HARD & SOFT
PORT3 HOL CONTROL REGISTER	0x0988~0x098C	HARD & SOFT
PORT4 HOL CONTROL REGISTER	0x0990~0x0994	HARD & SOFT
PORT5 HOL CONTROL REGISTER	0x0998~0x099C	HARD & SOFT
PORT6 HOL CONTROL REGISTER	0x09A0~0x09A4	HARD & SOFT

Table 3-151. **Parser Register Summary (continued)**

Name	Address	Reset
PORT0 FLOW CTRL THESHOLD REGISTER	0x09B0	HARD & SOFT
PORT1 FLOW CTRL THESHOLD REGISTER	0x09B4	HARD & SOFT
PORT2 FLOW CTRL THESHOLD REGISTER	0x09B8	HARD & SOFT
PORT3 FLOW CTRL THESHOLD REGISTER	0x09BC	HARD & SOFT
PORT4 FLOW CTRL THESHOLD REGISTER	0x09C0	HARD & SOFT
PORT5 FLOW CTRL THESHOLD REGISTER	0x09C4	HARD & SOFT
PORT6 FLOW CTRL THESHOLD REGISTER	0x09C8	HARD & SOFT
ACL POLICY MODE REGISTER	0x09F0	HARD & SOFT
ACL COUNTER MODE REGISTER	0x09F4	HARD & SOFT
ACL POLICY COUNTER RESET REGISTER	0x09F8	HARD & SOFT
ACL0 RATE LIMIT CONTROL REGISTER	0x0A00~0x0A04	HARD & SOFT
ACL1 RATE LIMIT CONTROL REGISTER	0x0A08~0x0A0C	HARD & SOFT
ACL2 RATE LIMIT CONTROL REGISTER	0x0A10~0x0A14	HARD & SOFT
ACL3 RATE LIMIT CONTROL REGISTER	0x0A18~0x0A1C	HARD & SOFT
ACL4 RATE LIMIT CONTROL REGISTER	0x0A20~0x0A24	HARD & SOFT
ACL5 RATE LIMIT CONTROL REGISTER	0x0A28~0x0A2C	HARD & SOFT

Table 3-151. **Parser Register Summary (continued)**

Name	Address	Reset
ACL6 RATE LIMIT CONTROL REGISTER	0x0A30~0x0A34	HARD & SOFT
ACL7 RATE LIMIT CONTROL REGISTER	0x0A38~0x0A3C	HARD & SOFT
ACL8 RATE LIMIT CONTROL REGISTER	0x0A40~0x0A44	HARD & SOFT
ACL9 RATE LIMIT CONTROL REGISTER	0x0A48~0x0A4C	HARD & SOFT
ACL10 RATE LIMIT CONTROL REGISTER	0x0A50~0x0A54	HARD & SOFT
ACL11 RATE LIMIT CONTROL REGISTER	0x0A58~0x0A5C	HARD & SOFT
ACL12 RATE LIMIT CONTROL REGISTER	0x0A60~0x0A64	HARD & SOFT
ACL13 RATE LIMIT CONTROL REGISTER	0x0A68~0x0A6C	HARD & SOFT
ACL14 RATE LIMIT CONTROL REGISTER	0x0A70~0x0A74	HARD & SOFT
ACL15 RATE LIMIT CONTROL REGISTER	0x0A78~0x0A7C	HARD & SOFT
ACL16 RATE LIMIT CONTROL REGISTER	0x0A80~0x0A84	HARD & SOFT
ACL17 RATE LIMIT CONTROL REGISTER	0x0A88~0x0A8C	HARD & SOFT
ACL18 RATE LIMIT CONTROL REGISTER	0x0A90~0x0A94	HARD & SOFT
ACL19 RATE LIMIT CONTROL REGISTER	0x0A98~0x0A9C	HARD & SOFT
ACL20 RATE LIMIT CONTROL REGISTER	0x0AA0~0x0AA4	HARD & SOFT

Table 3-151. **Parser Register Summary (continued)**

Name	Address	Reset
ACL21 RATE LIMIT CONTROL REGISTER	0x0AA8~0x0AAC	HARD & SOFT
ACL22 RATE LIMIT CONTROL REGISTER	0x0AB0~0x0AB4	HARD & SOFT
ACL23 RATE LIMIT CONTROL REGISTER	0x0AB8~0x0ABC	HARD & SOFT
ACL24 RATE LIMIT CONTROL REGISTER	0x0AC0~0x0AC4	HARD & SOFT
ACL25 RATE LIMIT CONTROL REGISTER	0x0AC8~0x0ACC	HARD & SOFT
ACL26 RATE LIMIT CONTROL REGISTER	0x0AD0~0x0AD4	HARD & SOFT
ACL27 RATE LIMIT CONTROL REGISTER	0x0AD8~0x0ADC	HARD & SOFT
ACL28 RATE LIMIT CONTROL REGISTER	0x0AE0~0x0AE4	HARD & SOFT
ACL29 RATE LIMIT CONTROL REGISTER	0x0AE8~0x0AEC	HARD & SOFT
ACL30 RATE LIMIT CONTROL REGISTER	0x0AF0~0x0AF4	HARD & SOFT
ACL31 RATE LIMIT CONTROL REGISTER	0x0AF8~0x0AFC	HARD & SOFT
PORT0 INGRESS RATE LIMIT CONTROL REGISTER	0x0B00~0x0B08	HARD & SOFT
PORT1 INGRESS RATE LIMIT CONTROL REGISTER	0x0B10~0x0B18	HARD & SOFT
PORT2 INGRESS RATE LIMIT CONTROL REGISTER	0x0B20~0x0B28	HARD & SOFT
PORT3 INGRESS RATE LIMIT CONTROL REGISTER	0x0B30~0x0B38	HARD & SOFT

Table 3-151. **Parser Register Summary (continued)**

Name	Address	Reset
PORT4 INGRESS RATE LIMIT CONTROL REGISTER	0x0B40~0x0B48	HARD & SOFT
PORT5 INGRESS RATE LIMIT CONTROL REGISTER	0x0B50~0x0B58	HARD & SOFT
PORT6 INGRESS RATE LIMIT CONTROL REGISTER	0x0B60~0x0B68	HARD & SOFT
TO CPU FRAME REMAP PRIORITY CONTROL REGISTER	0x0B70	HARD & SOFT

3.7.1 GLOBAL_FLOW_THD

0x0800

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Table 3-152, "Global Flow Control Register," on page 180 summarizes the GLOBAL_FLOW_THD Register

Table 3-152. **Global Flow Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:25	R/O	0	RESERVED	
24:16	R/W	'h120	GOL_XON_THRES	Global base transmit on threshold. When block memory used by all ports less than this value, mac would send out pause off frame, and link partner will start transmit frame out.
15:9	R/O	0	RESERVED	
8:0	R/W	'h188	GOL_XOFF_THRES	Global base transmit off threshold. When block memory used by all ports more than this value, mac would send out pause on frame, and link partner will stop transmit frame out.

3.7.2 QM_CTRL_REG

Address 0x0808

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Table 3-153, "QM Control Register," on page 181 summarizes the QM_CTRL_REG Register

Table 3-153. **QM Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29:28	R/O	0	RESERVED	
27:26	R/O	0	RESERVED	
25:24	R/O	0	RESERVED	
23:11	R/O	0	RESERVED	
10	R/W	0	QM_FUNC_TEST	1'b1: function test, qm should drop all packets from port1,2,3,4,5
9	R/W	0	MS_FC_EN	Multicast server flow control enable
8	R/O	0	RESERVED	
7	R/W	0	RATE_DROP_EN	drop packet enable due to rate limit. 1'b1: switch will drop frames due to rate limit. 1'b0: switch would use flow control to the source port due to rate limit, if the port won't stop switch will drop frame from that port.
6	R/W	0	FLOW_DROP_EN	1'b1: packet could be drop due to flow control except the highest priority packet. 1'b0: switch won't drop packets due to flow control
5:0	R/W	'hE	FLOW_DROP_CNT	Max free queue could be use after the port has been flow control. Then packets should be drop except the highest priori. Default value 'hE is set to normal packets which length is no more than 1518 bytes. For jumbo frame, 'd33 is commanded.

3.7.3 WAN_QUEUE_MAP_REG

Address 0x0810

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Table 3-154, "WAN Port PRI to Queue Mapping Register," on page 182 summarizes the WAN_QUEUE_MAP_REG Register

Table 3-154. **WAN Port PRI to Queue Mapping Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/W	0	WAN_PRI_QUEUE_0X7	The destination Queue for priority value 0x7 in port 0, 5 and 6
27	R/O	0	RESERVED	
26:24	R/W	0	WAN_PRI_QUEUE_0X6	The destination Queue for priority value 0x6 in port 0, 5 and 6
23	R/O	0	RESERVED	
22:20	R/W	0	WAN_PRI_QUEUE_0X5	The destination Queue for priority value 0x5 in port 0, 5 and 6
19	R/O	0	RESERVED	
18:16	R/W	0	WAN_PRI_QUEUE_0X4	The destination Queue for priority value 0x4 in port 0, 5 and 6
15	R/O	0	RESERVED	
14:12	R/W	0	WAN_PRI_QUEUE_0X3	The destination Queue for priority value 0x3 in port 0, 5 and 6
11	R/O	0	RESERVED	
10:8	R/W	0	WAN_PRI_QUEUE_0X2	The destination Queue for priority value 0x2 in port 0, 5 and 6
7	R/O	0	RESERVED	
6:4	R/W	0	WAN_PRI_QUEUE_0X1	The destination Queue for priority value 0x1 in port 0, 5 and 6

Bit	R/W	Inital Value	Mnemonic	Description
3	R/O	0	RESERVED	
2:0	R/W	0	WAN_PRI_QUEUE_0X0	The destination Queue for priority value 0x0 in port 0, 5 and 6

3.7.4 LAN_QUEUE_MAP_REG

Address 0x0814

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Table 3-155, "LAN Port PRI to Queue Mapping Register," on page 183 summarizes the LAN_QUEUE_MAP_REG Register

Table 3-155. **LAN Port PRI to Queue Mapping Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29:28	R/W	0	LAN_PRI_QUEUE_0X7	The destination Queue for priority value 0x7 in port 1, 2, 3 and 4
27:26	R/O	0	RESERVED	
25:24	R/W	0	LAN_PRI_QUEUE_0X6	The destination Queue for priority value 0x6 in port 1, 2, 3 and 4
23:22	R/O	0	RESERVED	
21:20	R/W	0	LAN_PRI_QUEUE_0X5LAN_PRI_QUEUE_0X5	The destination Queue for priority value 0x5 in port 1, 2, 3 and 4
19:18	R/O	0	RESERVED	
17:16	R/W	0	LAN_PRI_QUEUE_0X4	The destination Queue for priority value 0x4 in port 1, 2, 3 and 4
15:14	R/O	0	RESERVED	
13:12	R/W	0	LAN_PRI_QUEUE_0X3	The destination Queue for priority value 0x3 in port 1, 2, 3 and 4

Bit	R/W	Inital Value	Mnemonic	Description
11:10	R/O	0	RESERVED	
9:8	R/W	0	LAN_PRI_QUEUE_0X2	The destination Queue for priority value 0x2 in port 1, 2, 3 and 4
7:6	R/O	0	RESERVED	
5:4	R/W	0	LAN_PRI_QUEUE_0X1	The destination Queue for priority value 0x1 in port 1, 2, 3 and 4
3:2	R/O	0	RESERVED	
1:0	R/W	0	LAN_PRI_QUEUE_0X0	The destination Queue for priority value 0x0 in port 1, 2, 3 and 4

3.7.5 PORT0_WRR_CTRL

Address 0x0830

SFT&HW RST

Table 3-156, "Port 0 WRR Control Register," on page 184 summarizes the PORT0_WRR_CTRL Register

Table 3-156. **Port 0 WRR Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/W	2'b00	WEIGHT_PRI_CTRL_0	2'b00: strict priority 2'b01: only highest queue use strick priority, others use weighted fair queuing schme 2'b10: the highest two queues use strick priority, other two queues use weighted fair queuing schme. 2'b11: all queues use weighted fair queuing schme which defined in "WRR_PRI3/2/1/0".
29:25	R/O	8	WRR_PRI5_1	Wrr setting for priority 5
24:20	R/O	8	WRR_PRI4_1	Wrr setting for priority 4
19:15	R/W	8	WRR_PRI3_0	Wrr setting for priority 3
14:10	R/W	4	WRR_PRI2_0	Wrr setting for priority 2

Bit	R/W	Inital Value	Mnemonic	Description
9:5	R/W	2	WRR_PRI1_0	Wrr setting for priority 1
4:0	R/W	1	WRR_PRI0_0	Wrr setting for priority 0

3.7.6 PORT1_WRR_CTRL

Address 0x0834

SFT&HW RST

Table 3-157, "Port 1 Control Register," on page 185 summarizes the PORT1_WRR_CTRL Register

Table 3-157. **Port 1 Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/W	2'b00	WEIGHT_PRI_CTRL_1	2'b00: strict priority 2'b01: only highest queue use strick priority, others use weighted fair queuing schme 2'b10: the highest two queues use strick priority, other two queues use weighted fair queuing schme. 2'b11: all queues use weighted fair queuing schme which defined in "WRR_PRI3/2/1/0".
29:25	R/O	8	RESERVED	
24:20	R/O	8	RESERVED	
19:15	R/W	8	WRR_PRI3_1	Wrr setting for priority 3
14:10	R/W	4	WRR_PRI2_1	Wrr setting for priority 2
9:5	R/W	2	WRR_PRI1_1	Wrr setting for priority 1
4:0	R/W	1	WRR_PRI0_1	Wrr setting for priority 0

3.7.7 PORT2_WRR_CTRL SFT&HW RST

Address 0x0838

Table 3-158, "Port 2 WRR Control Register," on page 186 summarizes the PORT2_WRR_CTRL Register

Table 3-158. **Port 2 WRR Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/W	2'b00	WEIGHT_PRI_CTRL_2	2'b00: strict priority 2'b01: only highest queue use strick priority, others use weighted fair queuing schme 2'b10: the highest two queues use strick priority, other two queues use weighted fair queuing schme. 2'b11: all queues use weighted fair queuing schme which defined in "WRR_PRI3/2/1/0".
29:25	R/O	8	RESERVED	
24:20	R/O	8	RESERVED	
19:15	R/W	8	WRR_PRI3_2	Wrr setting for priority 3
14:10	R/W	4	WRR_PRI2_2	Wrr setting for priority 2
9:5	R/W	2	WRR_PRI1_2	Wrr setting for priority 1
4:0	R/W	1	WRR_PRI0_2	Wrr setting for priority 0

3.7.8 PORT3_WRR_CTRL

Address 0x083C

SFT&HW RST

Table 3-159, "Port 3 WRR Control Register," on page 187 summarizes the PORT3_WRR_CTRL Register

Table 3-159. **Port 3 WRR Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/W	2'b00	WEIGHT_PRI_CTRL_3	2'b00: strict priority 2'b01: only highest queue use strick priority, others use weighted fair queuing schme 2'b10: the highest two queues use strick priority, other two queues use weighted fair queuing schme. 2'b11: all queues use weighted fair queuing schme which defined in "WRR_PRI3/2/1/0".
29:25	R/W	8	RESERVED	
24:20	R/W	8	RESERVED	
19:15	R/W	8	WRR_PRI3_3	Wrr setting for priority 3
14:10	R/W	4	WRR_PRI2_3	Wrr setting for priority 2
9:5	R/W	2	WRR_PRI1_3	Wrr setting for priority 1
4:0	R/W	1	WRR_PRI0_3	Wrr setting for priority 0

3.7.9 PORT4_WRR_CTRL

Address 0x0840

SFT&HW RST

Table 3-160 summarizes the PORT4_WRR_CTRL Register

Table 3-160. **Port 4 WRR Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/W	2'b00	WEIGHT_PRI_CTRL_4	2'b00: strict priority 2'b01: only highest queue use strick priority, others use weighted fair queuing schme 2'b10: the highest two queues use strick priority, other two queues use weighted fair queuing schme. 2'b11: all queues use weighted fair queuing schme which defined in "WRR_PRI3/2/1/0".
29:25	R/O	8	RESERVED	
24:20	R/O	8	RESERVED	
19:15	R/W	8	WRR_PRI3_4	Wrr setting for priority 3
14:10	R/W	4	WRR_PRI2_4	Wrr setting for priority 2
9:5	R/W	2	WRR_PRI1_4	Wrr setting for priority 1
4:0	R/W	1	WRR_PRI0_4	Wrr setting for priority 0

3.7.10 PORT5_WRR_CTRL

Address 0x0844

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Table 3-161 summarizes the PORT5_WRR_CTRL Register

Table 3-161. **Port 5 WRR Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/W	2'b00	WEIGHT_PRI_CTRL_5	2'b00: strict priority 2'b01: only highest queue use strick priority, others use weighted fair queuing schme 2'b10: the highest two queues use strick priority, other two queues use weighted fair queuing schme. 2'b11: all queues use weighted fair queuing schme which defined in "WRR_PRI3/2/1/0".
29:25	R/W	8	WRR_PRI5_5	Wrr setting for priority 5
24:20	R/W	8	WRR_PRI4_5	Wrr setting for priority 4
19:15	R/W	8	WRR_PRI3_5	Wrr setting for priority 3
14:10	R/W	4	WRR_PRI2_5	Wrr setting for priority 2
9:5	R/W	2	WRR_PRI1_5	Wrr setting for priority 1
4:0	R/W	1	WRR_PRI0_5	Wrr setting for priority 0

3.7.11 PORT6_WRR_CTRL

Address 0x0848

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Table 3-162, "Port 6 WRR Control Register," on page 190 summarizes the PORT6_WRR_CTRL Register

Table 3-162. **Port 6 WRR Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/W	2'b00	WEIGHT_PRI_CTRL_6	2'b00: strict priority 2'b01: only highest queue use strick priority, others use weighted fair queuing schme 2'b10: the highest two queues use strick priority, other two queues use weighted fair queuing schme. 2'b11: all queues use weighted fair queuing schme which defined in "WRR_PRI3/2/1/0".
29:25	R/W	8	WRR_PRI5_6	Wrr setting for priority 5
24:20	R/W	8	WRR_PRI4_6	Wrr setting for priority 4
19:15	R/W	8	WRR_PRI3_6	Wrr setting for priority 3
14:10	R/W	4	WRR_PRI2_6	Wrr setting for priority 2
9:5	R/W	2	WRR_PRI1_6	Wrr setting for priority 1
4:0	R/W	1	WRR_PRI0_6	Wrr setting for priority 0

3.7.12 PORT0_EG_RATE_CTRL0

Address 0x0890

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Table 3-163, "Port 0 Rate Limit Control Register 0," on page 191 summarizes the PORT0_EG_RATE_CTRL0 Register 0

Table 3-163. **Port 0 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_0	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from por 0.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_0	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from port 0.

3.7.13 PORT0_EG_RATE_CTRL1

Address 0x0894

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Table 3-164, "Port 0 Rate Limit Control Register 1," on page 191 summarizes the PORT0_EG_RATE_CTRL1 Register 1

Table 3-164. **Port 0 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_0	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from port 0.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_0	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from port 0.

3.7.14 PORT0_EG_RATE_CTRL2

Address 0x0898

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Table 3-165, "Port 0 Rate Limit Control Register 2," on page 192 summarizes the PORT0_EG_RATE_CTRL2 Register 2

Table 3-165. **Port 0 Rate Limit Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_CIR_0	Egress Rate Limit for priority 5. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. if these bits are set to 15'h0, no priority 5 frame should be send out from port 0.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_CIR_0	Egress Rate Limit for priority 4. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. if these bits are set to 15'h0, no priority 4 frame should be send out from port 0.

3.7.15 PORT0_EG_RATE_CTRL3

Address 0x089C

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Table 3-166, "Port 0 Rate Limit Control Register 3," on page 193 summerizes the PORT0_EG_RATE_CTRL3 Register 3

Table 3-166. **Port 0 Rate Limit Control Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_0	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_0	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.16 PORT0_EG_RATE_CTRL4

Address 0x08A0

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Table 3-167, "Port 0 Rate Limit Control Register 4," on page 193 summarizes the PORT0_EG_RATE_CTRL4 Register 4

Table 3-167. **Port 0 Rate Limit Control Register 4**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_0	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR _0	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.17 PORT0_EG_RATE_CTRL5

Address 0x08A4

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Table 3-168, "Port 0 Rate Limit Control Register 5," on page 194 summerizes the PORT0_EG_RATE_CTRL5 Register 5

Table 3-168. **Port 0 Rate Limit Control Register 5**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_EIR _0	Egress Rate Limit for priority 5. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. if these bits are set to 15'h0, no priority 5 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_EIR_0	Egress Rate Limit for priority 4. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. if these bits are set to 15'h0, no priority 4 frame should be send out from this port.

3.7.18 PORT0_EG_RATE_CTRL6

Address 0x08A8

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Table 3-169 summerizes the PORT0_EG_RATE_CTRL6 Register 6

Table 3-169. **Port 0 Rate Limit Control Register 6**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_0	Committed burst size for priority 3 Commit Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
27	R/O	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_0	Excess burst size for priority 3 Excess Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets

Bit	R/W	Inital Value	Mnemonic	Description
23	R/O	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_0	Committed burst size for priority 2 Commit Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
19	R/O	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_0	Excess burst size for priority 2 Excess Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
15	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
14:12	R/W	0	EG_PRI1_CBS_0	Committed burst size for priority 1 Commit Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
11	R/O	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_0	Excess burst size for priority 1 Excess Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
7	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
6:4	R/W	0	EG_PRI0_CBS_0	Committed burst size for priority 0 Commit Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
3	R/O	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_0	Excess burst size for priority 0 Excess Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets

3.7.19 PORT0_EG_RATE_CTRL7 SFT&HW RST

Address 0x08AC

Table 3-170, "Port 0 Rate Limit Control Register 7," on page 199 summerizes the PORT0_EG_RATE_CTRL7 Register 7

Table 3-170. **Port 0 Rate Limit Control Register 7**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/W	0	EG_PRI5_CBS_0	Committed burst size for priority 5 Commit Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
27	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
26:24	R/W	0	EG_PRI5_EBS_0	Excess burst size for priority 5 Excess Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
23	R/O	0	RESERVED	
22:20	R/W	0	EG_PRI4_CBS_0	Committed burst size for priority 4 Commit Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
19	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
18:16	R/W	0	EG_PRI4_EBS_0	Excess burst size for priority 4 Excess Burst Size 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes for packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
15:14	R/O	0	RESERVED	
13	R/W	0	EG_PRI5_RATE_UNIT_0	Rate limit unit for queue 5: 1: Packets/ 0: bytes
12	R/W	0	EG_PRI4_RATE_UNIT_0	Rate limit unit for queue 4: 1: Packets/ 0: bytes
11	R/W	0	EG_PRI3_RATE_UNIT_0	Rate limit unit for queue 3: 1: Packets/ 0: bytes
10	R/W	0	EG_PRI2_RATE_UNIT_0	Rate limit unit for queue 2: 1: Packets/ 0: bytes
9	R/W	0	EG_PRI1_RATE_UNIT_0	Rate limit unit for queue 1: 1: Packets/ 0: bytes
8	R/W	0	EG_PRI0_RATE_UNIT_0	Rate limit unit for queue 0: 1: Packets/ 0: bytes
7:5	R/O	0	RESERVED	
4	R/W	0	EGRESS_MANAGE_RATE_EN_0	Enable management frame to be calculate to egress rate limit .

Bit	R/W	Inital Value	Mnemonic	Description
3	R/W	0	EGRESS_RATE_EN_0	Enable port base rate limit. Rate should be set at EG_PRIO_CIR Enable port-based max burst size also. Max burst size is set at EG_PRIO_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_0	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

3.7.20 PORT1_EG_RATE_CTRL0

Address 0x08B0

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Table 3-171, "Port 1 Rate Limit Control Register 0," on page 202 summarizes the PORT1_EG_RATE_CTRL0 Register 0

Table 3-171. **Port 1 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_1	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_1	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.21 PORT1_EG_RATE_CTRL0

Address 0x08B4

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Table 3-172, "Port 1 Rate Limit Control Register 0," on page 203 summarizes the PORT1_EG_RATE_CTRL0 Register 0

Table 3-172. **Port 1 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_1	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_1	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.22 PORT1_EG_RATE_CTRL3

Address 0x08BC

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Table 3-173, "Port 1 Rate Limit Control Register 3," on page 204 summerizes the PORT1_EG_RATE_CTRL3 Register 3

Table 3-173. **Port 1 Rate Limit Control Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_1	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_1	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.23 PORT1_EG_RATE_CTRL0

Address 0x08C0

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Table 3-174, "Port 1 Rate Limit Control Register 4," on page 204 summerizes the PORT1_EG_RATE_CTRL0 Register 4

Table 3-174. **Port 1 Rate Limit Control Register 4**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_1	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR _1	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.24 PORT1_EG_RATE_CTRL6

Address 0x08C8

SFT&HW RST

Table 3-175, "Port 1 Rate Limit Control Register 6," on page 205 summerizes the PORT1_EG_RATE_CTRL6 Register 6

Table 3-175. **Port 1 Rate Limit Control Register 6**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_1	Committed burst size for priority 3
27	R/O	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_1	Excess burst size for priority 3
23	R/O	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_1	Committed burst size for priority 2
19	R/O	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_1	Excess burst size for priority 2
15	R/O	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_1	Committed burst size for priority 1

Bit	R/W	Inital Value	Mnemonic	Description
11	R/O	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_1	Excess burst size for priority 1
7	R/O	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_1	Committed burst size for priority 0
3	R/O	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_1	Excess burst size for priority 0

3.7.25 PORT1_EG_RATE_CTRL7

Address 0x08CC

SFT&HW RST

Table 3-176, "Port 1 Rate Limit Control Register 7," on page 206 summerizes the PORT1_EG_RATE_CTRL7 Register 7

Table 3-176. **Port 1 Rate Limit Control Register 7**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:12	R/O	0	RESERVED	
11	R/W	0	EG_PRI3_RATE_UNIT_1	Rate limit unit for queue 3: 1: Packets/ 0: bytes
10	R/W	0	EG_PRI2_RATE_UNIT_1	Rate limit unit for queue 2: 1: Packets/ 0: bytes
9	R/W	0	EG_PRI1_RATE_UNIT_1	Rate limit unit for queue 1: 1: Packets/ 0: bytes
8	R/W	0	EG_PRI0_RATE_UNIT_1	Rate limit unit for queue 0: 1: Packets/ 0: bytes
7:5	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
4	R/W	0	EGRESS_MANAGE_RATE_EN_1	Enable management frame to be calculate to egress rate limit .
3	R/W	0	EGRESS_RATE_EN_1	Enable port-based rate limit. Rate is set at EG_PRIO_CIR Enable port-based max burst size also. Max burst size is set at EG_PRIO_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_1	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

3.7.26 PORT2_EG_RATE_CTRL0

Address 0x08D0

SFT&HW RST

Table 3-177, "Port 2 Rate Limit Control Register 0," on page 207 summerizes the PORT2_EG_RATE_CTRL0 Register 0

Table 3-177. **Port 2 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_2	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_2	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.27 PORT2_EG_RATE_CTRL0

Address 0x08D4

SFT&HW RST

Table 3-178, "Port 2 Rate Limit Control Register 1," on page 208 summarizes the PORT2_EG_RATE_CTRL0 Register 1

Table 3-178. **Port 2 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_2	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_2	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.28 PORT2_EG_RATE_CTRL0

Address 0x08DC

SFT&HW RST

Table 3-179, "Port 2 Rate Limit Control Register 3," on page 209 summarizes the PORT2_EG_RATE_CTRL0 Register 3

Table 3-179. **Port 2 Rate Limit Control Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_2	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_2	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.29 PORT2_EG_RATE_CTRL0

Address 0x08E0

SFT&HW RST

Table 3-180, "Port 2 Rate Limit Control Register 4," on page 209 summarizes the PORT2_EG_RATE_CTRL0 Register 4

Table 3-180. **Port 2 Rate Limit Control Register 4**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_2	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR _2	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.30 PORT2_EG_RATE_CTRL0

Address 0x08E8

SFT&HW RST

Table 3-181, "Port 2 Rate Limit Control Register 6," on page 210 summarizes the PORT2_EG_RATE_CTRL0 Register 6

Table 3-181. **Port 2 Rate Limit Control Register 6**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_2	Committed burst size for priority 3
27	R/O	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_2	Excess burst size for priority 3
23	R/O	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_2	Committed burst size for priority 2
19	R/O	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_2	Excess burst size for priority 2
15	R/O	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_2	Committed burst size for priority 1

Bit	R/W	Inital Value	Mnemonic	Description
11	R/O	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_2	Excess burst size for priority 1
7	R/O	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_2	Committed burst size for priority 0
3	R/O	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_2	Excess burst size for priority 0

3.7.31 PORT2_EG_RATE_CTRL0

Address 0x08EC

SFT&HW RST

Table 3-182, "Port 2 Rate Limit Control Register 7," on page 211 summarizes the PORT2_EG_RATE_CTRL0 Register 7

Table 3-182. **Port 2 Rate Limit Control Register 7**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:12	R/O	0	RESERVED	
11	R/W	0	EG_PRI3_RATE_UNIT_2	Rate limit unit for queue 3: 1: Packets/ 0: bytes
10	R/W	0	EG_PRI2_RATE_UNIT_2	Rate limit unit for queue 2: 1: Packets/ 0: bytes
9	R/W	0	EG_PRI1_RATE_UNIT_2	Rate limit unit for queue 1: 1: Packets/ 0: bytes
8	R/W	0	EG_PRI0_RATE_UNIT_2	Rate limit unit for queue 0: 1: Packets/ 0: bytes
7:5	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
4	R/W	0	EGRESS_MANAGE_RATE_EN_2	Enable management frame to be calculate to egress rate limit .
3	R/W	0	EGRESS_RATE_EN_2	Enable port-based rate limit. Rate is set at EG_PRIO_CIR Max burst size is also set at EG_PRIO_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_2	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

3.7.32 PORT3_EG_RATE_CTRL0

Address 0x08F0

SFT&HW RST

Table 3-183, "Port 3 Rate Limit Control Register 0," on page 212 summarizes the PORT3_EG_RATE_CTRL0 Register 0

Table 3-183. **Port 3 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_3	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_3	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.33 PORT3_EG_RATE_CTRL0

Address 0x08F4

SFT&HW RST

Table 3-184, "Port 3 Rate Limit Control Register 1," on page 213 summarizes the PORT3_EG_RATE_CTRL0 Register 1

Table 3-184. **Port 3 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_3	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_3	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.34 PORT3_EG_RATE_CTRL2

Address 0x08FC

SFT&HW RST

Table 3-185, "Port 3 Rate Limit Control Register 3," on page 214 summarizes the PORT3_EG_RATE_CTRL2 Register 3

Table 3-185. **Port 3 Rate Limit Control Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_3	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_3	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.35 PORT3_EG_RATE_CTRL2

Address 0x0900

SFT&HW RST

Table 3-186, "Port 3 Rate Limit Control Register 4," on page 214 summarizes the PORT3_EG_RATE_CTRL2 Register 4

Table 3-186. **Port 3 Rate Limit Control Register 4**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_3	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR _3	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.36 PORT3_EG_RATE_CTRL5

Address 0x0908

SFT&HW RST

Table 3-187, "Port 3 Rate Limit Control Register 6," on page 215 summariazes the PORT3_EG_RATE_CTRL5 Register 6

Table 3-187. **Port 3 Rate Limit Control Register 6**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_3	Committed burst size for priority 3
27	R/O	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_3	Excess burst size for priority 3
23	R/O	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_3	Committed burst size for priority 2
19	R/O	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_3	Excess burst size for priority 2
15	R/O	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_3	Committed burst size for priority 1

Bit	R/W	Inital Value	Mnemonic	Description
11	R/O	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_3	Excess burst size for priority 1
7	R/O	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_3	Committed burst size for priority 0
3	R/O	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_3	Excess burst size for priority 0

3.7.37 PORT3_EG_RATE_CTRL5

Address 0x090C

SFT&HW RST

Table 3-188, "Port 3 Rate Limit Control Register 7," on page 216 summariazes the PORT3_EG_RATE_CTRL5 Register 7

Table 3-188. **Port 3 Rate Limit Control Register 7**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:12	R/O	0	RESERVED	
11	R/W	0	EG_PRI3_RATE_UNIT_3	Rate limit unit for queue 3: 1: Packets/ 0: bytes
10	R/W	0	EG_PRI2_RATE_UNIT_3	Rate limit unit for queue 2: 1: Packets/ 0: bytes
9	R/W	0	EG_PRI1_RATE_UNIT_3	Rate limit unit for queue 1: 1: Packets/ 0: bytes
8	R/W	0	EG_PRI0_RATE_UNIT_3	Rate limit unit for queue 0: 1: Packets/ 0: bytes
7:5	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
4	R/W	0	EGRESS_MANAGE_RATE_EN_3	Enable management frame to be calculate to egress rate limit .
3	R/W	0	EGRESS_RATE_EN_3	Enable port-based rate limit. Rate is set at EG_PRIO_CIR Enable Max burst size also. Max burst size is set at EG_PRIO_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_3	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

3.7.38 PORT4_EG_RATE_CTRL5

Address 0x0910

SFT&HW RST

Table 3-189, "Port 4 Rate Limit Control Register 0," on page 217 summariazes the PORT4_EG_RATE_CTRL5 Register 0

Table 3-189. **Port 4 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_4	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_4	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.39 PORT4_EG_RATE_CTRL5

Address 0x0914

SFT&HW RST

Table 3-190, "Port 4 Rate Limit Control Register 1," on page 218 summariazes the PORT4_EG_RATE_CTRL5 Register 1

Table 3-190. **Port 4 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_4	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_4	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.40 PORT4_EG_RATE_CTRL5

Address 0x091C

SFT&HW RST

Table 3-191, "Port 4 Rate Limit Control Register 3," on page 219 summariazes the PORT4_EG_RATE_CTRL5 Register 3

Table 3-191. **Port 4 Rate Limit Control Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_4	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_4	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.41 PORT4_EG_RATE_CTRL5

Address 0x0920

SFT&HW RST

Table 3-192, "Port 4 Rate Limit Control Register 4," on page 219 summariazes the PORT4_EG_RATE_CTRL5 Register 4

Table 3-192. **Port 4 Rate Limit Control Register 4**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_4	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR _4	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.42 PORT4_EG_RATE_CTRL6

Address 0x0928

SFT&HW RST

Table 3-193, "Port 4 Rate Limit Control Register 6," on page 220 summarizes the PORT4_EG_RATE_CTRL6 Register 6

Table 3-193. **Port 4 Rate Limit Control Register 6**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_4	Committed burst size for priority 3
27	R/O	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_4	Excess burst size for priority 3
23	R/O	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_4	Committed burst size for priority 2
19	R/O	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_4	Excess burst size for priority 2
15	R/O	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_4	Committed burst size for priority 1

Bit	R/W	Inital Value	Mnemonic	Description
11	R/O	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_4	Excess burst size for priority 1
7	R/O	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_4	Committed burst size for priority 0
3	R/O	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_4	Excess burst size for priority 0

3.7.43 PORT4_EG_RATE_CTRL7

Address 0x092C

SFT&HW RST

Table 3-194, "Port 4 Rate Limit Control Register 7," on page 221 summarizes the PORT4_EG_RATE_CTRL7 Register 7

Table 3-194. **Port 4 Rate Limit Control Register 7**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/O	0	RESERVED	
11	R/W	0	EG_PRI3_RATE_UNIT_4	Rate limit unit for queue 3: 1: Packets/ 0: bytes
10	R/W	0	EG_PRI2_RATE_UNIT_4	Rate limit unit for queue 2: 1: Packets/ 0: bytes
9	R/W	0	EG_PRI1_RATE_UNIT_4	Rate limit unit for queue 1: 1: Packets/ 0: bytes
8	R/W	0	EG_PRI0_RATE_UNIT_4	Rate limit unit for queue 0: 1: Packets/ 0: bytes
7:5	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
4	R/W	0	EGRESS_MANAGE_RATE_EN_4	Enable management frame to be calculate to egress rate limit .
3	R/W	0	EGRESS_RATE_EN_4	Enable port-based rate limit. Rate is set at EG_PRIO_CBS Enable Max burst size also. Max burst size is set at EG_PRIO_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_4	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

3.7.44 PORT5_EG_RATE_CTRL0

Address 0x0930

SFT&HW RST

Table 3-195, "Port 5 Rate Limit Control Register 0," on page 222 summarizes the PORT5_EG_RATE_CTRL0 Register 0

Table 3-195. **Port 5 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_5	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_5	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.45 PORT5_EG_RATE_CTRL1

Address 0x0934

SFT&HW RST

Table 3-196, "Port 5 Rate Limit Control Register 1," on page 223 summarizes the PORT5_EG_RATE_CTRL1 Register 1

Table 3-196. **Port 5 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_5	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_5	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.46 PORT5_EG_RATE_CTRL2

Address 0x0938

SFT&HW RST

Table 3-197, "Port 5 Rate Limit Control Register 2," on page 224 summarizes the PORT5_EG_RATE_CTRL2 Register 2

Table 3-197. **Port 5 Rate Limit Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_CIR_5	Egress Rate Limit for priority 5. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. if these bits are set to 15'h0, no priority 5 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_CIR_5	Egress Rate Limit for priority 4. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. if these bits are set to 15'h0, no priority 4 frame should be send out from this port.

3.7.47 PORT5_EG_RATE_CTRL3

Address 0x093C

SFT&HW RST

Table 3-198, "Port 5 Rate Limit Control Register 3," on page 224 Port 5 Rate Limit Control Register 3

Table 3-198. **Port 5 Rate Limit Control Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_5	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_5	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.48 PORT5_EG_RATE_CTRL4

Address 0x0940

SFT&HW RST

Table 3-199, "Port 5 Rate Limit Control Register 4," on page 225 summarizes the PORT5_EG_RATE_CTRL4 Register 4

Table 3-199. **Port 5 Rate Limit Control Register 4**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_5	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR _5	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.49 PORT5_EG_RATE_CTRL5

Address 0x0944

SFT&HW RST

Table 3-200, "Port 5 Rate Limit Control Register 5," on page 226 summarizes the PORT5_EG_RATE_CTRL5 Register 5

Table 3-200. **Port 5 Rate Limit Control Register 5**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_EIR _5	Egress Rate Limit for priority 5. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. if these bits are set to 15'h0, no priority 5 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_EIR_5	Egress Rate Limit for priority 4 Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. if these bits are set to 15'h0, no priority 4 frame should be send out from this port.

3.7.50 PORT5_EG_RATE_CTRL6

Address 0x0948

SFT&HW RST

Table 3-201, "Port 5 Rate Limit Control Register 6," on page 226 summarizes the PORT5_EG_RATE_CTRL6 Register 6

Table 3-201. **Port 5 Rate Limit Control Register 6**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_5	Committed burst size for priority 3
27	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
26:24	R/W	0	EG_PRI3_EBS_5	Excess burst size for priority 3
23	R/O	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_5	Committed burst size for priority 2
19	R/O	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_5	Excess burst size for priority 2
15	R/O	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_5	Committed burst size for priority 1
11	R/O	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_5	Excess burst size for priority 1
7	R/O	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_5	Committed burst size for priority 0
3	R/O	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_5	Excess burst size for priority 0

3.7.51 PORT5_EG_RATE_CTRL7

Address 0x094C

SFT&HW RST

Table 3-202, "Port 5 Rate Limit Control Register 7," on page 228 summarizes the PORT5_EG_RATE_CTRL7 Register 7

Table 3-202. **Port 5 Rate Limit Control Register 7**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/W	0	EG_PRI5_CBS_5	Committed burst size for priority 5
27	R/O	0	RESERVED	
26:24	R/W	0	EG_PRI5_EBS_5	Excess burst size for priority 5
23	R/O	0	RESERVED	
22:20	R/W	0	EG_PRI4_CBS_5	Committed burst size for priority 4
19	R/O	0	RESERVED	
18:16	R/W	0	EG_PRI4_EBS_5	Excess burst size for priority 4
15:14	R/O	0	RESERVED	
13	R/W	0	EG_PRI5_RATE_UNIT_5	Rate limit unit for queue 5: 1: Packets/ 0: bytes
12	R/W	0	EG_PRI4_RATE_UNIT_5	Rate limit unit for queue 4: 1: Packets/ 0: bytes
11	R/W	0	EG_PRI3_RATE_UNIT_5	Rate limit unit for queue 3: 1: Packets/ 0: bytes
10	R/W	0	EG_PRI2_RATE_UNIT_5	Rate limit unit for queue 2: 1: Packets/ 0: bytes
9	R/W	0	EG_PRI1_RATE_UNIT_5	Rate limit unit for queue 1: 1: Packets/ 0: bytes
8	R/W	0	EG_PRI0_RATE_UNIT_5	Rate limit unit for queue 0: 1: Packets/ 0: bytes
7:5	R/O	0	RESERVED	
4	R/W	0	EGRESS_MANAGE_RATE_EN_5	Enable management frame to be calculate to egress rate limit .

Bit	R/W	Inital Value	Mnemonic	Description
3	R/W	0	EGRESS_RATE_EN_5	Enable port-based rate limit. Rate is set at EG_PRIO_CIR Enable Max burst size also. Max burst size is set at EG_PRIO_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_5	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

3.7.52 PORT6_EG_RATE_CTRL0

Address 0x0950

SFT&HW RST

Table 3-203, "Port 6 Rate Limit Control Register 0," on page 229 summarizes the PORT6_EG_RATE_CTRL0 Register 0

Table 3-203. **Port 6 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_6	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_6	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.53 PORT6_EG_RATE_CTRL1

Address 0x0954

SFT&HW RST

Table 3-204, "Port 6 Rate Limit Control Register 1," on page 230 summarizes the PORT6_EG_RATE_CTRL1 Register 1

Table 3-204. **Port 6 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_6	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_6	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.54 PORT6_EG_RATE_CTRL2

Address 0x0958

SFT&HW RST

Table 3-205, "Port 6 Rate Limit Control Register 2," on page 231 summarizes the PORT6_EG_RATE_CTRL2 Register 2

Table 3-205. **Port 6 Rate Limit Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_CIR_6	Egress Rate Limit for priority 5. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. if these bits are set to 15'h0, no priority 5 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_CIR_6	Egress Rate Limit for priority 4. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. if these bits are set to 15'h0, no priority 4 frame should be send out from this port.

3.7.55 PORT6_EG_RATE_CTRL3

Address 0x095C

SFT&HW RST

Table 3-206, "Port 6 Rate Limit Control Register 3," on page 231 summarizes the PORT6_EG_RATE_CTRL3 Register 3

Table 3-206. **Port 6 Rate Limit Control Register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_6	Egress Rate Limit for priority 1. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. if these bits are set to 15'h0, no priority 1 frame should be send out from this port.

Bit	R/W	Inital Value	Mnemonic	Description
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_6	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. if these bits are set to 15'h0, no priority 0 frame should be send out from this port.

3.7.56 PORT6_EG_RATE_CTRL4

Address 0x0960

SFT&HW RST

Table 3-207, "Port 6 Rate Limit Control Register 4," on page 232 summarizes the PORT6_EG_RATE_CTRL4 Register 4

Table 3-207. **Port 6 Rate Limit Control Register 4**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_6	Egress Rate Limit for priority 3. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. if these bits are set to 15'h0, no priority 3 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR _6	Egress Rate Limit for priority 2. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no priority 2 frame should be send out from this port.

3.7.57 PORT6_EG_RATE_CTRL5

Address 0x0964

SFT&HW RST

Table 3-208, "Port 6 Rate Limit Control Register 5," on page 233 summarizes the PORT6_EG_RATE_CTRL5 Register 5

Table 3-208. **Port 6 Rate Limit Control Register 5**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_EIR _6	Egress Rate Limit for priority 5. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. if these bits are set to 15'h0, no priority 5 frame should be send out from this port.
15	R/O	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_EIR_6	Egress Rate Limit for priority 4. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. if these bits are set to 15'h0, no priority 4 frame should be send out from this port.

3.7.58 PORT6_EG_RATE_CTRL6

Address 0x0968

SFT&HW RST

Table 3-209, "Port 6 Rate Limit Control Register 6," on page 233 summerizes the PORT6_EG_RATE_CTRL6 Register 6

Table 3-209. **Port 6 Rate Limit Control Register 6**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_6	Committed burst size for priority 3
27	R/O	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_6	Excess burst size for priority 3

Bit	R/W	Inital Value	Mnemonic	Description
23	R/O	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_6	Committed burst size for priority 2
19	R/O	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_6	Excess burst size for priority 2
15	R/O	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_6	Committed burst size for priority 1
11	R/O	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_6	Excess burst size for priority 1
7	R/O	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_6	Committed burst size for priority 0
3	R/O	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_6	Excess burst size for priority 0

3.7.59 PORT6_EG_RATE_CTRL6

Address 0x096C

SFT&HW RST

Table 3-210, "Port 6 Rate Limit Control Register 7," on page 234 summerizes the PORT6_EG_RATE_CTRL6 Register 7

Table 3-210. **Port 6 Rate Limit Control Register 7**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0	RESERVED	
30:28	R/W	0	EG_PRI5_CBS_6	Committed burst size for priority 5
27	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
26:24	R/W	0	EG_PRI5_EBS_6	Excess burst size for priority 5
23	R/O	0	RESERVED	
22:20	R/W	0	EG_PRI4_CBS_6	Committed burst size for priority 4
19	R/O	0	RESERVED	
18:16	R/W	0	EG_PRI4_EBS_6	Excess burst size for priority 4
15:14	R/O	0	RESERVED	
13	R/W	0	EG_PRI5_RATE_UNIT_6	Rate limit unit for queue 5: 1: Packets/ 0: bytes
12	R/W	0	EG_PRI4_RATE_UNIT_6	Rate limit unit for queue 4: 1: Packets/ 0: bytes
11	R/O	0	EG_PRI3_RATE_UNIT_6	Rate limit unit for queue 3: 1: Packets/ 0: bytes
10	R/W	0	EG_PRI2_RATE_UNIT_6	Rate limit unit for queue 2: 1: Packets/ 0: bytes
9	R/W	0	EG_PRI1_RATE_UNIT_6	Rate limit unit for queue 1: 1: Packets/ 0: bytes
8	R/W	0	EG_PRI0_RATE_UNIT_6	Rate limit unit for queue 0: 1: Packets/ 0: bytes
7:5	R/O	0	RESERVED	
4	R/W	0	EGRESS_MANAGE_RATE_EN_6	Enable management frame to be calculate to egress rate limit .

Bit	R/W	Inital Value	Mnemonic	Description
3	R/O	0	EGRESS_RATE_EN_6	Enable Port-based rate limit. Rate is set at EG_PRIO_CIR Enable Port-based Max burst size also. Max burst size is set at EG_PRIO_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_6	Egress rate limit time slot control register. 3'h0? 1/128 ms 3'h1? 1/64 ms 3'h2? 1/32 ms 3'h3? 1/16 ms 3'h4? 1/4 ms 3'h5? 1 ms 3'h6? 10 ms 3'h7? 100 ms

3.7.60 PORT0_HOL_CTRL0

Address 0x0970

SFT&HW RST

Table 3-211, "Port 0 HOL Control Register 0," on page 236 summerizes the PORT0_HOL_CTRL0 Register 0

Table 3-211. **Port 0 HOL Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_0	Most buffer can be used for this port. Buffer number is times of 4. 6'h0: 0 6'h1: no more than 4 6'h2: no more than 8 …… 6'h3F: no more than 252
23:20	R/W	0x8	EG_PRI5_QUEUE_NUM_0	See bit [3:0]. This is for priority queue 5.
19:16	R/W	0x8	EG_PRI4_QUEUE_NUM_0	See bit [3:0]. This is for priority queue 4.
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_0	See bit [3:0]. This is for priority queue 3.

Bit	R/W	Inital Value	Mnemonic	Description
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_0	See bit [3:0]. This is for priority queue 2.
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_0	See bit [3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_0	Most buffer can be used for priority 0 queue. Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.61 PORT0_HOL_CTRL1

Address 0x0974

SFT&HW RST

Table 3-212, "Port 0 HOL Control Register 1," on page 237 summerizes the PORT0_HOL_CTRL1 Register 1

Table 3-212. **Port 0 HOL Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:17	R/O	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_0	Egress port mirror. If this bit is set to 1'b1, all packets send out through this port should be copied to mirror port.
15:8	R/O	0	RESERVED	
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_0	1'b1: enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_0	1'b1: enable use PRI*_QUEUE_NUM to control queue depth in this port.

Bit	R/W	Inital Value	Mnemonic	Description
5:4	R/O	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_0	Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.62 PORT1_HOL_CTRL0

Address 0x0978

SFT&HW RST

Table 3-213, "Port 1 HOL Control Register 0," on page 238 summerizes the PORT1_HOL_CTRL0 Register 0

Table 3-213. **Port 1 HOL Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_1	Most buffer can be used for this port. Buffer number is times of 4. 6'h0: 0 6'h1: no more than 4 6'h2: no more than 8 …… 6'h3F: no more than 252
23:20	R/W	0	RESERVED	
19:16	R/W	0	RESERVED	
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_1	See bit [3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_1	See bit [3:0]. This is for priority queue 2.

Bit	R/W	Inital Value	Mnemonic	Description
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_1	See bit [3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_1	Most buffer can be used for priority 0 queue. Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.63 PORT1_HOL_CTRL1

Address 0x097C

SFT&HW RST

Table 3-214, "Port 1 HOL Control Register 1," on page 239 summerizes the PORT1_HOL_CTRL1 Register 1

Table 3-214. **Port 1 HOL Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:17	R/O	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_1	Egress port mirror. If this bit is set to 1'b1, all packets send out through this port should be copied to mirror port.
15:8	R/O	0	RESERVED	
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_1	1'b1: enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_1	1'b1: enable use PRI*_QUEUE_NUM to control queue depth in this port.

Bit	R/W	Inital Value	Mnemonic	Description
5:4	R/O	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_1	Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.64 PORT2_HOL_CTRL0

Address 0x0980

SFT&HW RST

Table 3-215, "Port 2 HOL Control Register 0," on page 240 summerizes the PORT2_HOL_CTRL0 Register 0

Table 3-215. **Port 2 HOL Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_2	Most buffer can be used for this port. Buffer number is times of 4. 6'h0: 0 6'h1: no more than 4 6'h2: no more than 8 …… 6'h3F: no more than 252
23:20	R/W	0x8	RESERVED	
19:16	R/W	0x8	RESERVED	
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_2	See bit [3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_2	See bit [3:0]. This is for priority queue 2.

Bit	R/W	Inital Value	Mnemonic	Description
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_2	See bit [3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_2	Most buffer can be used for priority 0 queue. Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.65 PORT2_HOL_CTRL1

Address 0x0984

SFT&HW RST

Table 3-216, "Port 2 HOL Control Register 1," on page 241 summerizes the PORT2_HOL_CTRL1 Register 1

Table 3-216. **Port 2 HOL Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:17	R/O	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_2	Egress port mirror. If this bit is set to 1'b1, all packets send out through this port should be copied to mirror port.
15:8	R/O	0	RESERVED	
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_2	1'b1: enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_2	1'b1: enable use PRI*_QUEUE_NUM to control queue depth in this port.

Bit	R/W	Inital Value	Mnemonic	Description
5:4	R/O	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_2	Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.66 PORT3_HOL_CTRL0

Address 0x0988

SFT&HW RST

Table 3-217, "Port 3 HOL Control Register 0," on page 242 summerizes the PORT3_HOL_CTRL0 Register 0

Table 3-217. **Port 3 HOL Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_3	Most buffer can be used for this port. Buffer number is times of 4. 6'h0: 0 6'h1: no more than 4 6'h2: no more than 8 …… 6'h1F: no more than 252
23:20	R/W	0x8	RESERVED	
19:16	R/W	0x8	RESERVED	
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_3	See bit [3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_3	See bit [3:0]. This is for priority queue 2.

Bit	R/W	Inital Value	Mnemonic	Description
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_3	See bit [3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_3	Most buffer can be used for priority 0 queue. Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.67 PORT3_HOL_CTRL1

Address 0x098C

SFT&HW RST

Table 3-218, "Port 3 HOL Control Register 1," on page 243 summerizes the PORT3_HOL_CTRL1 Register 1

Table 3-218. **Port 3 HOL Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:17	R/O	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_3	Egress port mirror. If this bit is set to 1'b1, all packets send out through this port should be copied to mirror port.
15:8	R/O	0	RESERVED	
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_3	1'b1: enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_3	1'b1: enable use PRI*_QUEUE_NUM to control queue depth in this port.

Bit	R/W	Inital Value	Mnemonic	Description
5:4	R/O	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_3	Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.68 PORT4_HOL_CTRL0

Address 0x0990

SFT&HW RST

Table 3-219, "Port 4 HOL Control Register 0," on page 244 summerizes the PORT4_HOL_CTRL0 Register 0

Table 3-219. **Port 4 HOL Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_4	Most buffer can be used for this port. Buffer number is times of 4. 6'h0: 0 6'h1: no more than 4 6'h2: no more than 8 …… 6'h3F: no more than 252
23:20	R/W	0x8	RESERVED	
19:16	R/W	0x8	RESERVED	
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_4	See bit [3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_4	See bit [3:0]. This is for priority queue 2.

Bit	R/W	Inital Value	Mnemonic	Description
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_4	See bit [3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_4	Most buffer can be used for priority 0 queue. Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.69 PORT4_HOL_CTRL1

Address 0x0994

SFT&HW RST

Table 3-220, "Port 4 HOL Control Register 1," on page 245 summerizes the PORT4_HOL_CTRL1 Register 1

Table 3-220. **Port 4 HOL Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:17	R/O	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_4	Egress port mirror. If this bit is set to 1'b1, all packets send out through this port should be copied to mirror port.
15:8	R/O	0	RESERVED	
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_4	1'b1: enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_4	1'b1: enable use PRI*_QUEUE_NUM to control queue depth in this port.

Bit	R/W	Inital Value	Mnemonic	Description
5:4	R/O	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_4	Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.70 PORT5_HOL_CTRL0

Address 0x0998

SFT&HW RST

Table 3-221, "Port 5 HOL Control Register 0," on page 246 Port 5 HOL Control summerizes the PORT5_HOL_CTRL0 Register 0

Table 3-221. **Port 5 HOL Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_5	Most buffer can be used for this port. Buffer number is times of 4. 6'h0: 0 6'h1: no more than 4 6'h2: no more than 8 …… 6'h3F: no more than 252
23:20	R/W	0x8	EG_PRI5_QUEUE_NUM_5	See bit [3:0]. This is for priority queue 5.
19:16	R/W	0x8	EG_PRI4_QUEUE_NUM_5	See bit [3:0]. This is for priority queue 4.
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_5	See bit [3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_5	See bit [3:0]. This is for priority queue 2.

Bit	R/W	Inital Value	Mnemonic	Description
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_5	See bit [3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_5	Most buffer can be used for priority 0 queue. Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.71 PORT5_HOL_CTRL1

Address 0x099C

SFT&HW RST

Table 3-222, "Port 5 HOL Control Register 1," on page 247 summerizes the PORT5_HOL_CTRL1 Register 1

Table 3-222. **Port 5 HOL Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:17	R/O	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_5	Egress port mirror. If this bit is set to 1'b1, all packets send out through this port should be copied to mirror port.
15:8	R/O	0	RESERVED	
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_5	1'b1: enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_5	1'b1: enable use PRI*_QUEUE_NUM to control queue depth in this port.

Bit	R/W	Inital Value	Mnemonic	Description
5:4	R/O	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_5	Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.72 PORT6_HOL_CTRL0

Address 0x09A0

SFT&HW RST

Table 3-223, "Port 6 HOL Control Register 0," on page 248 summerizes the PORT6_HOL_CTRL0 Register 0

Table 3-223. **Port 6 HOL Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/O	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_6	Most buffer can be used for this port. Buffer number is times of 4. 6'h0: 0 6'h1: no more than 4 6'h2: no more than 8 …… 6'h3F: no more than 252
23:20	R/W	0x8	EG_PRI5_QUEUE_NUM_6	See bit [3:0]. This is for priority queue 5.
19:16	R/W	0x8	EG_PRI4_QUEUE_NUM_6	See bit [3:0]. This is for priority queue 4.
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_6	See bit [3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_6	See bit [3:0]. This is for priority queue 2.

Bit	R/W	Inital Value	Mnemonic	Description
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_6	See bit [3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_6	Most buffer can be used for priority 0 queue. Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.73 PORT6_HOL_CTRL1

Address 0x09A4

SFT&HW RST

Table 3-224, "Port 6 HOL Control Register 1," on page 249 summerizes the PORT6_HOL_CTRL1 Register 1

Table 3-224. **Port 6 HOL Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:17	R/O	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_6	Egress port mirror. If this bit is set to 1'b1, all packets send out through this port should be copied to mirror port.
15:8	R/O	0	RESERVED	
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_6	1'b1: enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_6	1'b1: enable use PRI*_QUEUE_NUM to control queue depth in this port.

Bit	R/W	Inital Value	Mnemonic	Description
5:4	R/O	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_6	Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.7.74 PORT0_FLOW_THD

Address 0x09B0

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Table 3-225, "Port 0 Flow Control Threshold Control Register," on page 250 summerizes the PORT0_FLOW_THD Register

Table 3-225. **Port 0 Flow Control Threshold Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_0	Port base transmit on threshold. When block memory used by one port less than this value, mac would send out pause off frame, and link partner will start transmit frame out.
15:8	R/O	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_0	Port base transmit off threshold. When block memory used by one port more than this value, mac would send out pause on frame, and link partner will stop transmit frame out.

3.7.75 PORT1_FLOW_THD

Address 0x09B4

SFT&HW RST

Table 3-226, "Port 1 Flow Control Threshold Control Register," on page 251 summerizes the PORT1_FLOW_THD Register

Table 3-226. **Port 1 Flow Control Threshold Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_1	Port base transmit on threshold. When block memory used by one port less than this value, mac would send out pause off frame, and link partner will start transmit frame out.
15:8	R/O	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_1	Port base transmit off threshold. When block memory used by one port more than this value, mac would send out pause on frame, and link partner will stop transmit frame out.

3.7.76 PORT2_FLOW_THD

Address 0x09B8

SFT&HW RST

Table 3-227, "Port 2 Flow Control Threshold Control Register," on page 251 Port 2 Flow Control Threshold Register

Table 3-227. **Port 2 Flow Control Threshold Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_2	Port base transmit on threshold. When block memory used by one port less than this value, mac would send out pause off frame, and link partner will start transmit frame out.
15:8	R/O	0	RESERVED	
7:0	R/W	'h4B	PORT_XOFF_THRES_2	Port base transmit off threshold. When block memory used by one port more than this value, mac would send out pause on frame, and link partner will stop transmit frame out.

3.7.77 PORT3_FLOW_THD

Address 0x09BC

SFT&HW RST

Table 3-228, "Port 3 Flow Control Threshold Control Register," on page 252 summerizes the PORT3_FLOW_THD Register

Table 3-228. **Port 3 Flow Control Threshold Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_3	Port base transmit on threshold. When block memory used by one port less than this value, mac would send out pause off frame, and link partner will start transmit frame out.
15:8	R/O	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_3	Port base transmit off threshold. When block memory used by one port more than this value, mac would send out pause on frame, and link partner will stop transmit frame out.

3.7.78 PORT4_FLOW_THD

Address 0x09C0

SFT&HW RST

Table 3-229, "Port 4 Flow Control Threshold Control Register," on page 252 summerizes the PORT4_FLOW_THD Register

Table 3-229. **Port 4 Flow Control Threshold Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_4	Port base transmit on threshold. When block memory used by one port less than this value, mac would send out pause off frame, and link partner will start transmit frame out.

Bit	R/W	Inital Value	Mnemonic	Description
15:8	R/O	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_4	Port base transmit off threshold. When block memory used by one port more than this value, mac would send out pause on frame, and link partner will stop transmit frame out.

3.7.79 PORT5_FLOW_THD

Address 0x09C4

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Table 3-230, "Port 5 Flow Control Threshold Control Register," on page 253 summerizes the PORT5_FLOW_THD Register

Table 3-230. **Port 5 Flow Control Threshold Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_5	Port base transmit on threshold. When block memory used by one port less than this value, mac would send out pause off frame, and link partner will start transmit frame out.
15:8	R/O	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_5	Port base transmit off threshold. When block memory used by one port more than this value, mac would send out pause on frame, and link partner will stop transmit frame out.

3.7.80 PORT6_FLOW_THD

Address 0x09C8

SFT&HW RST

Table 3-231, "Port 6 Flow Control Threshold Control Register," on page 254 summerizes the PORT6_FLOW_THD Register

Table 3-231. **Port 6 Flow Control Threshold Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_6	Port base transmit on threshold. When block memory used by one port less than this value, mac would send out pause off frame, and link partner will start transmit frame out.
15:8	R/O	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_6	Port base transmit off threshold. When block memory used by one port more than this value, mac would send out pause on frame, and link partner will stop transmit frame out.

3.7.81 ACL_POLICY_MODE

Address 0x09F0

SFT&HW RST

Table 3-232, "ACL Policy Register," on page 254 summarizes the ACL_POLICY_MODE Register

Table 3-232. **ACL Policy Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	ACL_SEL_31	See bit [0]
30	R/W	0	ACL_SEL_30	See bit [0]
29	R/W	0	ACL_SEL_29	See bit [0]
28	R/W	0	ACL_SEL_28	See bit [0]
27	R/W	0	ACL_SEL_27	See bit [0]
26	R/W	0	ACL_SEL_26	See bit [0]
25	R/W	0	ACL_SEL_25	See bit [0]

Bit	R/W	Inital Value	Mnemonic	Description
24	R/W	0	ACL_SEL_24	See bit [0]
23	R/W	0	ACL_SEL_23	See bit [0]
22	R/W	0	ACL_SEL_22	See bit [0]
21	R/W	0	ACL_SEL_21	See bit [0]
20	R/W	0	ACL_SEL_20	See bit [0]
19	R/W	0	ACL_SEL_19	See bit [0]
18	R/W	0	ACL_SEL_18	See bit [0]
17	R/W	0	ACL_SEL_17	See bit [0]
16	R/W	0	ACL_SEL_16	See bit [0]
15	R/W	0	ACL_SEL_15	See bit [0]
14	R/W	0	ACL_SEL_14	See bit [0]
13	R/W	0	ACL_SEL_13	See bit [0]
12	R/W	0	ACL_SEL_12	See bit [0]
11	R/W	0	ACL_SEL_11	See bit [0]
10	R/W	0	ACL_SEL_10	See bit [0]
9	R/W	0	ACL_SEL_9	See bit [0]
8	R/W	0	ACL_SEL_8	See bit [0]
7	R/W	0	ACL_SEL_7	See bit [0]
6	R/W	0	ACL_SEL_6	See bit [0]
5	R/W	0	ACL_SEL_5	See bit [0]
4	R/W	0	ACL_SEL_4	See bit [0]

Bit	R/W	Inital Value	Mnemonic	Description
3	R/W	0	ACL_SEL_3	See bit [0]
2	R/W	0	ACL_SEL_2	See bit [0]
1	R/W	0	ACL_SEL_1	See bit [0]
0	R/W	0	ACL_SEL_0	1:ACL COUNTER 0:ACL RATE LIMIT

3.7.82 ACL_COUNTER_MODE

Address 0x09F4

SFT&HW RST

Table 3-233, "ACL Counter Mode Register," on page 256 summerizes the ACL_COUNTER_MODE Register

Table 3-233. **ACL Counter Mode Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	ACL_CNT_MODE_31	See bit [0]
30	R/W	0	ACL_CNT_MODE_30	See bit [0]
29	R/W	0	ACL_CNT_MODE_29	See bit [0]
28	R/W	0	ACL_CNT_MODE_28	See bit [0]
27	R/W	0	ACL_CNT_MODE_27	See bit [0]
26	R/W	0	ACL_CNT_MODE_26	See bit [0]
25	R/W	0	ACL_CNT_MODE_25	See bit [0]
24	R/W	0	ACL_CNT_MODE_24	See bit [0]
23	R/W	0	ACL_CNT_MODE_23	See bit [0]
22	R/W	0	ACL_CNT_MODE_22	See bit [0]

Bit	R/W	Inital Value	Mnemonic	Description
21	R/W	0	ACL_CNT_MODE_21	See bit [0]
20	R/W	0	ACL_CNT_MODE_20	See bit [0]
19	R/W	0	ACL_CNT_MODE_19	See bit [0]
18	R/W	0	ACL_CNT_MODE_18	See bit [0]
17	R/W	0	ACL_CNT_MODE_17	See bit [0]
16	R/W	0	ACL_CNT_MODE_16	See bit [0]
15	R/W	0	ACL_CNT_MODE_15	See bit [0]
14	R/W	0	ACL_CNT_MODE_14	See bit [0]
13	R/W	0	ACL_CNT_MODE_13	See bit [0]
12	R/W	0	ACL_CNT_MODE_12	See bit [0]
11	R/W	0	ACL_CNT_MODE_11	See bit [0]
10	R/W	0	ACL_CNT_MODE_10	See bit [0]
9	R/W	0	ACL_CNT_MODE_9	See bit [0]
8	R/W	0	ACL_CNT_MODE_8	See bit [0]
7	R/W	0	ACL_CNT_MODE_7	See bit [0]
6	R/W	0	ACL_CNT_MODE_6	See bit [0]
5	R/W	0	ACL_CNT_MODE_5	See bit [0]
4	R/W	0	ACL_CNT_MODE_4	See bit [0]
3	R/W	0	ACL_CNT_MODE_3	See bit [0]
2	R/W	0	ACL_CNT_MODE_2	See bit [0]

Bit	R/W	Inital Value	Mnemonic	Description
1	R/W	0	ACL_CNT_MODE_1	See bit [0]
0	R/W	0	ACL_CNT_MODE_0	1:BYTE Country 0:FRAME Counter

3.7.83 ACL_CNT_RESET

Address 0x09F8

SFT&HW RST

Table 3-234, "ACL Counter Reset Register," on page 258 summerizes the ACL_CNT_RESET Register

Table 3-234. **ACL Counter Reset Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	ACL_CNT_RST_31	See bit [0]
30	R/W	0	ACL_CNT_RST_30	See bit [0]
29	R/W	0	ACL_CNT_RST_29	See bit [0]
28	R/W	0	ACL_CNT_RST_28	See bit [0]
27	R/W	0	ACL_CNT_RST_27	See bit [0]
26	R/W	0	ACL_CNT_RST_26	See bit [0]
25	R/W	0	ACL_CNT_RST_25	See bit [0]
24	R/W	0	ACL_CNT_RST_24	See bit [0]
23	R/W	0	ACL_CNT_RST_23	See bit [0]
22	R/W	0	ACL_CNT_RST_22	See bit [0]
21	R/W	0	ACL_CNT_RST_21	See bit [0]
20	R/W	0	ACL_CNT_RST_20	See bit [0]

Bit	R/W	Inital Value	Mnemonic	Description
19	R/W	0	ACL_CNT_RST_19	See bit [0]
18	R/W	0	ACL_CNT_RST_18	See bit [0]
17	R/W	0	ACL_CNT_RST_17	See bit [0]
16	R/W	0	ACL_CNT_RST_16	See bit [0]
15	R/W	0	ACL_CNT_RST_15	See bit [0]
14	R/W	0	ACL_CNT_RST_14	See bit [0]
13	R/W	0	ACL_CNT_RST_13	See bit [0]
12	R/W	0	ACL_CNT_RST_12	See bit [0]
11	R/W	0	ACL_CNT_RST_11	See bit [0]
10	R/W	0	ACL_CNT_RST_10	See bit [0]
9	R/W	0	ACL_CNT_RST_9	See bit [0]
8	R/W	0	ACL_CNT_RST_8	See bit [0]
7	R/W	0	ACL_CNT_RST_7	See bit [0]
6	R/W	0	ACL_CNT_RST_6	See bit [0]
5	R/W	0	ACL_CNT_RST_5	See bit [0]
4	R/W	0	ACL_CNT_RST_4	See bit [0]
3	R/W	0	ACL_CNT_RST_3	See bit [0]
2	R/W	0	ACL_CNT_RST_2	See bit [0]
1	R/W	0	ACL_CNT_RST_1	See bit [0]
0	R/W	0	ACL_CNT_RST_0	1.clear the counter

3.7.84 ACL_RATE_CTRL0 Address 0x0A00

SFT&HW RST

Table 3-235, "ACL_0 Rate Limit Register 0," on page 260 summerizes the ACL_RATE_CTRL0 Register 0

Table 3-235. **ACL_0 Rate Limit Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_0	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_0	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.85 ACL_RATE_CTRL1_0

Address 0x0A04

SFT&HW RST

Table 3-236, "ACL_0 Rate Control Register 1," on page 260 summerizes the ACL_RATE_CTRL1_0 Register 1

Table 3-236. **ACL_0 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_0	Borrow enable
22	R/W	0	ACL_RATE_UNIT_0	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_0	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_0	Color mode for ingress rate limit

Bit	R/W	Inital Value	Mnemonic	Description
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_0	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_0	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_0	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.86 ACL_RATE_CTRL0_1

Address 0x0A08

SFT&HW RST

Table 3-237, "ACL Rate Control Register 0," on page 261 summerizes the ACL_RATE_CTRL0_1 Register 0

Table 3-237. **ACL Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_1	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_1	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.87 ACL_RATE_CTRL1_1

SFT&HW RST

Address 0x0A0C

Table 3-238, "ACL_1 Rate Control Register 1," on page 262 summerizes the ACL_RATE_CTRL1_1 Register 1

Table 3-238. **ACL_1 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_1	Borrow enable
22	R/W	0	ACL_RATE_UNIT_1	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_1	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_1	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_1	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_1	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_1	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.88 ACL_RATE_CTRL0_2

Address 0x0A10

SFT&HW RST

Table 3-239, "ACL_2 Rate Control Register 0," on page 263 summerizes the ACL_RATE_CTRL0_2 Register 0

Table 3-239. **ACL_2 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_2	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_2	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.89 ACL_RATE_CTRL1_2

Address 0x0A14

SFT&HW RST

Table 3-240, "ACL_2 Rate Control Register 1," on page 263 summerizes the ACL_RATE_CTRL1_2 Register 1

Table 3-240. **ACL_2 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_2	Borrow enable
22	R/W	0	ACL_RATE_UNIT_2	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_2	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_2	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_2	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_EBS_2	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_2	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.90 ACL_RATE_CTRL0_3

Address 0x0A18

SFT&HW RST

Table 3-241, "ACL_3 Rate Control Register 0," on page 264 summerizes the ACL_RATE_CTRL0_3 Register 0

Table 3-241. **ACL_3 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_3	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_3	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.91 ACL_RATE_CTRL1_3

Address 0x0A1C

SFT&HW RST

Table 3-242, "ACL_3 Rate Control Register 1," on page 265 summerizes the ACL_RATE_CTRL1_3 Register 1

Table 3-242. **ACL_3 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_3	Borrow enable
22	R/W	0	ACL_RATE_UNIT_3	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_3	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_3	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_3	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_3	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_3	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.92 ACL_RATE_CTRL0_4

Address 0x0A20

SFT&HW RST

Table 3-243, "ACL_4 Rate Control Register 0," on page 266 summerizes the ACL_RATE_CTRL0_4 Register 0

Table 3-243. **ACL_4 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_4	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_4	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.93 ACL_RATE_CTRL1_4

Address 0x0A24

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Table 3-244, "ACL_4 Rate Control Register," on page 266 ACL_4 rate control Register 1

Table 3-244. **ACL_4 Rate Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_4	Borrow enable
22	R/W	0	ACL_RATE_UNIT_4	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_4	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_4	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_4	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_EBS_4	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_4	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.94 ACL_RATE_CTRL1_5

Address 0x0A28

SFT&HW RST

Table 3-245, "ACL_5 Rate Control Register," on page 267 summerizes the ACL_RATE_CTRL1_5 Register 1

Table 3-245. **ACL_5 Rate Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_5	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_5	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.95 ACL_RATE_CTRL1_5

Address 0x0A2C

SFT&HW RST

Table 3-246, "ACL_5 Rate Control Register 1," on page 267 summerizes the ACL_RATE_CTRL1_5 Register 1

Table 3-246. **ACL_5 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_5	Borrow enable

Bit	R/W	Inital Value	Mnemonic	Description
22	R/W	0	ACL_RATE_UNIT_5	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_5	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_5	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_5	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_5	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_5	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.96 ACL_RATE_CTRL0_6

Address 0x0A30

SFT&HW RST

Table 3-247, "ACL_6 Rate Control Register 0," on page 268 summerizes the ACL_RATE_CTRL0_6 Register 0

Table 3-247. **ACL_6 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_6	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_6	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.97 ACL_RATE_CTRL1_6

SFT&HW RST

Address 0x0A34

Table 3-248, "ACL_6 Rate Control Register 0," on page 269 summerizes the ACL_RATE_CTRL1_6 Register 0

Table 3-248. **ACL_6 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_6	Borrow enable
22	R/W	0	ACL_RATE_UNIT_6	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_6	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_6	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_6	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_6	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_6	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.98 ACL_RATE_CTRL1_7

Address 0x0A38

SFT&HW RST

Table 3-249, "ACL_7 Rate Limit Control Register 1," on page 269 summerizes the ACL_RATE_CTRL1_7 Register 1

Table 3-249. **ACL_7 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_CBS_7	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_7	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.99 ACL_RATE_CTRL1_7

Address 0x0A3C

SFT&HW RST

Table 3-250, "ACL_7 Rate Control Register 1," on page 270 summerizes the ACL_RATE_CTRL1_7 Register 1

Table 3-250. **ACL_7 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_7	Borrow enable
22	R/W	0	ACL_RATE_UNIT_7	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_7	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_7	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_7	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_7	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_7	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.100 ACL_RATE_CTRL0_8

SFT&HW RST

Address 0x0A40

Table 3-251, "ACL_8 Rate Control Register 0," on page 271 summerizes the ACL_RATE_CTRL0_8 Register 0

Table 3-251. **ACL_8 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_8	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_8	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.101 ACL_RATE_CTRL1_8

Address 0x0A44

SFT&HW RST)

Table 3-252, "ACL_8 Rate Control Register 1," on page 271 summerizes the ACL_RATE_CTRL1_8 Register 1

Table 3-252. **ACL_8 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_8	Borrow enable
22	R/W	0	ACL_RATE_UNIT_8	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_8	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_8	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_8	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_EBS_8	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_8	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.102 ACL_RATE_CTRL0_9

Address 0x0A48

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Table 3-253, "ACL_9 Rate Control Register 0," on page 272 summerizes the ACL_RATE_CTRL0_9 Register 0

Table 3-253. **ACL_9 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_9	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_9	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.103 ACL_RATE_CTRL1_9

Address 0x0A4C

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Table 3-254, "ACL_9 Rate Control Register 1," on page 273 summerizes the ACL_RATE_CTRL1_9 Register 1

Table 3-254. **ACL_9 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_9	Borrow enable
22	R/W	0	ACL_RATE_UNIT_9	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_9	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_9	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_9	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_9	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_9	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.104 ACL_RATE_CTRL0_10

Address 0x0A50

SFT&HW RST

Table 3-255, "ACL_10 Rate Control Register 0," on page 273 summerizes the ACL_RATE_CTRL0_10 Register 0

Table 3-255. **ACL_10 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_10	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_10	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.105 ACL_RATE_CTRL0_10

Address 0x0A54

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Table 3-256, "ACL_10 Rate Control Register 1," on page 274 summerizes the ACL_RATE_CTRL0_10 Register 1

Table 3-256. **ACL_10 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_10	Borrow enable
22	R/W	0	ACL_RATE_UNIT_10	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_10	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_10	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_10	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_10	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_10	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.106 ACL_RATE_CTRL0_11

Address 0x0A58

SFT&HW RST

Table 3-257, "ACL_11 Rate Control Register 0," on page 275 summerizes the ACL_RATE_CTRL0_11 Register 0

Table 3-257. **ACL_11 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_11	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_11	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.107 ACL_RATE_CTRL1_11

Address 0x0A5C

FT&HW RST

Table 3-258, "ACL_11 Rate Control Register 1," on page 275 summerizes the ACL_RATE_CTRL1_11 Register 1

Table 3-258. **ACL_11 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_11	Borrow enable
22	R/W	0	ACL_RATE_UNIT_11	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_11	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_11	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_11	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_11	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_11	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.108 ACL_RATE_CTRL0_12

Address 0x0A60

SFT&HW RST

Table 3-259, "ACL_12 Rate Control Register 0," on page 276 summerizes the ACL_RATE_CTRL0_12 Register 0

Table 3-259. **ACL_12 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_12	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_12	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.109 ACL_RATE_CTRL1_12

Address 0x0A64

SFT&HW RST

Table 3-260, "ACL_12 Rate Control Register 1," on page 276 summerizes the ACL_RATE_CTRL1_12Register 1

Table 3-260. **ACL_12 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_12	Borrow enable
22	R/W	0	ACL_RATE_UNIT_12	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_12	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_12	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_12	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_EBS_12	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_12	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.110 ACL_RATE_CTRL0_13

Address 0x0A68

SFT&HW RST

Table 3-261, "ACL_13 Rate Control Register 0," on page 277 summerizes the ACL_RATE_CTRL0_13 Register 0

Table 3-261. **ACL_13 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_13	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_13	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.111 ACL_RATE_CTRL1_13

Address 0x0A6C

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Table 3-262, "ACL_13 Rate Control Register 1," on page 277 summerizes the ACL_RATE_CTRL1_13 Register 1

Table 3-262. **ACL_13 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_13	Borrow enable

Bit	R/W	Inital Value	Mnemonic	Description
22	R/W	0	ACL_RATE_UNIT_13	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_13	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_13	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_13	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_13	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_13	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.112 ACL_RATE_CTRL0_14

Address 0x0A70

SFT&HW RST

Table 3-263, "ACL_14 Rate Control Register 0," on page 278 summerizes the ACL_RATE_CTRL0_14 Register 0

Table 3-263. **ACL_14 Rate Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_14	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_14	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.113 ACL_RATE_CTRL1_14

Address 0x0A74

SFT&HW RST

Table 3-264, "ACL_14 Rate Control Register 1," on page 279 summerizes the ACL_RATE_CTRL1_14 Register 1

Table 3-264. **ACL_14 Rate Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_14	Borrow enable
22	R/W	0	ACL_RATE_UNIT_14	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_14	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_14	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_14	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_14	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_14	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.114 ACL_RATE_CTRL0_15

Address 0x0A78

SFT&HW RST

Table 3-265, "ACL_15 Rate Limit Control Register 0," on page 279 summerizes the ACL_RATE_CTRL0_15 Register 0

Table 3-265. **ACL_15 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_CBS_15	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_15	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.115 ACL_RATE_CTRL1_15

Address 0x0A7C

SFT&HW RST

Table 3-266, "ACL_15 Rate Limit Control Register 1," on page 280 summerizes the ACL_RATE_CTRL1_15 Register 1

Table 3-266. **ACL_15 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_15	Borrow enable
22	R/W	0	ACL_RATE_UNIT_15	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_15	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_15	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_15	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_15	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_15	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.116 ACL_RATE_CTRL1_16

Address 0x0A80

SFT&HW RST

Table 3-267, "ACL_16 Rate Limit Control Register 0," on page 281 summerizes the ACL_RATE_CTRL1_16 Register 0

Table 3-267. **ACL_16 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_16	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_16	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.117 ACL_RATE_CTRL1_16

Address 0x0A84

SFT&HW RST

Table 3-268, "ACL_16 Rate Limit Control Register 1," on page 281 summerizes the ACL_RATE_CTRL1_16 Register 1

Table 3-268. **ACL_16 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_16	Borrow enable
22	R/W	0	ACL_RATE_UNIT_16	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_16	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_16	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_16	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_EBS_16	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_16	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.118 ACL_RATE_CTRL1_17

Address 0x0A88

SFT&HW RST

Table 3-269, "ACL_17 Rate Limit Control Register 0," on page 282 summerizes the ACL_RATE_CTRL1_17 Register 0

Table 3-269. **ACL_17 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_17	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_17	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.119 ACL_RATE_CTRL1_17

Address 0x0A8C

SFT&HW RST

Table 3-270, "ACL_17 Rate Limit Control Register 1," on page 283 summerizes the ACL_RATE_CTRL1_17 Register 1

Table 3-270. **ACL_17 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_17	Borrow enable
22	R/W	0	ACL_RATE_UNIT_17	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_17	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_17	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_17	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_17	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_17	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.120 ACL_RATE_CTRL0_18

Address 0x0A90

SFT&HW RST

Table 3-271, "ACL_18 Rate Limit Control Register 0," on page 283 summerizes the ACL_RATE_CTRL0_18 Register 0

Table 3-271. **ACL_18 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_18	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_18	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.121 ACL_RATE_CTRL0_18

Address 0x0A94

SFT&HW RST

Table 3-272, "ACL_18 Rate Limit Control Register 1," on page 284 summerizes the ACL_RATE_CTRL0_18 Register 1

Table 3-272. **ACL_18 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_18	Borrow enable
22	R/W	0	ACL_RATE_UNIT_18	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_18	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_18	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_18	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_18	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_18	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.122 ACL_RATE_CTRL0_19

Address 0x0A98

SFT&HW RST

Table 3-273, "ACL_19 Rate Limit Control Register 0," on page 285 summerizes the ACL_RATE_CTRL0_19 Register 0

Table 3-273. **ACL_19 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_19	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_19	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.123 ACL_RATE_CTRL1_19

Address 0x0A9C

SFT&HW RST

Table 3-274, "ACL_19 Rate Limit Control Register 1," on page 285 summerizes the ACL_RATE_CTRL1_19 Register 1

Table 3-274. **ACL_19 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_19	Borrow enable
22	R/W	0	ACL_RATE_UNIT_19	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_19	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_19	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_19	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_19	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_19	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.124 ACL_RATE_CTRL1_20

Address 0x0AA0

SFT&HW RST

Table 3-275, "ACL_20 Rate Limit Control Register 0," on page 286 summerizes the ACL_RATE_CTRL1_20 Register 0

Table 3-275. **ACL_20 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_20	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_20	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.125 ACL_RATE_CTRL1_20

Address 0x0AA4

SFT&HW RST

Table 3-276, "ACL_20 Rate Limit Control Register 1," on page 286 summerizes the ACL_RATE_CTRL1_20 Register 1

Table 3-276. **ACL_20 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_20	Borrow enable
22	R/W	0	ACL_RATE_UNIT_20	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_20	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_20	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_20	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_EBS_20	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_20	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.126 ACL_RATE_CTRL0_21

Address 0x0AA8

SFT&HW RST

Table 3-277, "ACL_21 Rate Limit Control Register 0," on page 287 summerizes the ACL_RATE_CTRL0_21 Register 0

Table 3-277. **ACL_21 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_21	Commited burst size for ingress rate limit
14:0	R/W	0	ACL_CIR_21	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.127 ACL_RATE_CTRL1_21

Address 0x0AAC

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Table 3-278, "ACL_21 Rate Limit Control Register 1," on page 288 summerizes the ACL_RATE_CTRL1_21 Register 1

Table 3-278. **ACL_21 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_21	Borrow enable
22	R/W	0	ACL_RATE_UNIT_21	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_21	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_21	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_21	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_21	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_21	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.128 ACL_RATE_CTRL0_22

Address 0x0AB0

SFT&HW RST

Table 3-279, "ACL_22 Rate Limit Control Register 0," on page 288 summerizes the ACL_RATE_CTRL0_2 Register 0

Table 3-279. **ACL_22 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_22	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_22	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.129 ACL_RATE_CTRL1_22

Address 0x0AB4

SFT&HW RST

Table 3-280, "ACL_22 Rate Limit Control Register 1," on page 289 summerizes the ACL_RATE_CTRL1_22 Register 1

Table 3-280. **ACL_22 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_22	Borrow enable
22	R/W	0	ACL_RATE_UNIT_22	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_22	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_22	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_22	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_22	Excess burst size for ingress rate limit
14:0	R/W	0X7FFF	ACL_EIR_22	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.130 ACL_RATE_CTRL0_23

Address 0x0AB8

SFT&HW RST

Table 3-281, "ACL_23 Rate Limit Control Register 0," on page 290 summerizes the ACL_RATE_CTRL0_23 Register 0

Table 3-281. **ACL_23 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_23	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_23	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.131 ACL_RATE_CTRL1_23

Address 0x0ABC

SFT&HW RST

Table 3-282, "ACL_23 Rate Limit Control Register 1," on page 290 summerizes the ACL_RATE_CTRL1_23 Register 1

Table 3-282. **ACL_23 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_23	Borrow enable
22	R/W	0	ACL_RATE_UNIT_23	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_23	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_23	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_23	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_23	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_23	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.132 ACL_RATE_CTRL0_24

Address 0x0AC0

SFT&HW RST

Table 3-283, "ACL_24 Rate Limit Control Register 0," on page 291 summerizes the ACL_RATE_CTRL0_24 Register 0

Table 3-283. **ACL_24 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_24	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_24	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.133 ACL_RATE_CTRL1_24

Address 0x0AC4

SFT&HW RST

Table 3-284, "ACL_24 Rate Limit Control Register 1," on page 291 summerizes the ACL_RATE_CTRL1_24 Register 1

Table 3-284. **ACL_24 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_24	Borrow enable
22	R/W	0	ACL_RATE_UNIT_24	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_24	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_24	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_24	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_EBS_24	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_24	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.134 ACL_RATE_CTRL0_25

Address 0x0AC8

SFT&HW RST

Table 3-285, "ACL_25 Rate Limit Control Register 0," on page 292 summerizes the ACL_RATE_CTRL0_25 Register 0

Table 3-285. **ACL_25 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_25	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_25	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.135 ACL_RATE_CTRL1_25

Address 0x0ACC

SFT&HW RST

Table 3-286, "ACL_25 Rate Limit Control Register 1," on page 292 summerizes the ACL_RATE_CTRL1_25 Register 1

Table 3-286. **ACL_25 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_25	Borrow enable

Bit	R/W	Inital Value	Mnemonic	Description
22	R/W	0	ACL_RATE_UNIT_25	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_25	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_25	Color mode for ingress rate limit
19:18	R/O	2'b01	ACL_RATE_TIME_SLOT_25	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_25	Excess burst size for ingress rate limit
14:0	R/O	0x7FFF	ACL_EIR_25	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.136 ACL_RATE_CTRL0_26

Address 0x0AD0

SFT&HW RST

Table 3-287, "ACL_26 Rate Limit Control Register 0," on page 293 summerizes the ACL_RATE_CTRL0_26 Register 0

Table 3-287. **ACL_26 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_26	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_26	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.137 ACL_RATE_CTRL1_26

Address 0x0AD4

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Table 3-288, "ACL_26 Rate Limit Control Register 1," on page 294 summerizes the ACL_RATE_CTRL1_26 Register 1

Table 3-288. **ACL_26 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_26	Borrow enable
22	R/W	0	ACL_RATE_UNIT_26	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_26	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_26	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_26	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_26	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_26	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.138 ACL_RATE_CTRL0_27

Address 0x0AD8

SFT&HW RST

Table 3-289, "ACL_27 Rate Limit Control Register 0," on page 294 summerizes the ACL_RATE_CTRL0_27 Register 0

Table 3-289. **ACL_27 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_CBS_27	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_27	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.139 ACL_RATE_CTRL1_27

Address 0x0ADC

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Table 3-290, "ACL_27 Rate Limit Control Register 1," on page 295 summerizes the ACL_RATE_CTRL1_27 Register 1

Table 3-290. **ACL_27 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_27	Borrow enable
22	R/W	0	ACL_RATE_UNIT_27	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_27	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_27	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_27	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_27	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_27	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.140 ACL_RATE_CTRL0_28

SFT&HW RST

Address 0x0AE0

Table 3-291, "ACL_28 Rate Limit Control Register 0," on page 296 summerizes the ACL_RATE_CTRL0_28 Register 0

Table 3-291. **ACL_28 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_28	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_28	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.141 ACL_RATE_CTRL1_28

Address 0x0AE4

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Table 3-292, "ACL_28 Rate Limit Control Register 1," on page 296 summerizes the ACL_RATE_CTRL1_28 Register 1

Table 3-292. **ACL_28 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_28	Borrow enable
22	R/W	0	ACL_RATE_UNIT_28	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_28	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_28	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_28	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_EBS_28	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_28	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.142 ACL_RATE_CTRL0_29

Address 0x0AE8

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Table 3-293, "ACL_29 Rate Limit Control Register 0," on page 297 summerizes the ACL_RATE_CTRL0_29 Register 0

Table 3-293. **ACL_29 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_29	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_29	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.143 ACL_RATE_CTRL1_29

Address 0x0AEC

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Table 3-294, "ACL_29 Rate Limit Control Register 1," on page 297 summerizes the ACL_RATE_CTRL1_29 Register 1

Table 3-294. **ACL_29 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_29	Borrow enable

Bit	R/W	Inital Value	Mnemonic	Description
22	R/W	0	ACL_RATE_UNIT_29	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_29	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_29	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_29	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_29	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_29	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.144 ACL_RATE_CTRL0_30

Address 0x0AF0

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Table 3-295, "ACL_30 Rate Limit Control Register 0," on page 298 summerizes the ACL_RATE_CTRL0_30 Register 0

Table 3-295. **ACL_30 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	
17:15	R/W	0	ACL_CBS_30	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_30	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.145 ACL_RATE_CTRL1_30

Address 0x0AF4

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Table 3-296, "ACL_30 Rate Limit Control Register 1," on page 299 summerizes the ACL_RATE_CTRL1_30 Register 1

Table 3-296. **ACL_30 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_30	Borrow enable
22	R/W	0	ACL_RATE_UNIT_30	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_30	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_30	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_30	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot
17:15	R/W	0	ACL_EBS_30	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_30	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.146 ACL_RATE_CTRL0_31

Address 0x0AF8

SFT&HW RST

Table 3-297, "ACL_31 Rate Limit Control Register 0," on page 299 summerizes the ACL_RATE_CTRL0_31 Register 0

Table 3-297. **ACL_31 Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_CBS_31	Commited burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_31	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.147 ACL_RATE_CTRL1_31

Address 0x0AFC

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Table 3-298, "ACL_31 Rate Limit Control Register 1," on page 300 summerizes the ACL_RATE_CTRL1_31 Register 1

Table 3-298. **ACL_31 Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_31	Borrow enable
22	R/W	0	ACL_RATE_UNIT_31	1: Packets/ 0: bytes
21	R/W	0	ACL_CF_31	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_31	Color mode for ingress rate limit
19:18	R/W	2'b01	ACL_RATE_TIME_SLOT_31	ACL Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ACL_EBS_31	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_31	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.148 PORT0_ING_RATE_CTRL0

Address 0x0B00

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Table 3-299, "Port 0 Ingress Rate Limit Control Register 0," on page 301 summerizes the PORT0_ING_RATE_CTRL0 Register 0

Table 3-299. **Port 0 Ingress Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_0	Byte number should be added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, crc and SFD.
23:22	R/W	2'b01	ING_RATE_C_TIME_SLOT_0	Committed Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
21	R/O	0	RESERVED	
20	R/W	0	ING_RATE_MODE_0	1: one two-rate three-color 0: two single rate
19:18	R/O	0	RESERVED	
17:15	/W	0	ING_CBS_0	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_0	Committed Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.149 PORT0_ING_RATE_CTRL1

Address 0x0B04

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Table 3-300, "Port 0 Ingress Rate Limit Control Register 1," on page 302 Port 0 Ingress Rate Limit Controlsummerizes the Register 1

Table 3-300. **Port 0 Ingress Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ING_BORROW_EN_0	Borrow enable
22	R/W	0	ING_RATE_UNIT_0	1: Packets/ 0: bytes
21	R/W	0	ING_CF_0	Coupling flag for ingress rate limit
20	R/W	0	ING_CM_0	Color mode for ingress rate limit
19:18	R/W	2'b01	ING_RATE_E_TIME_SLOT_0	Excess Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
17:15	R/W	0	ING_EBS_0	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_0	Excess Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.150 PORT0_ING_RATE_CTRL2

Address 0x0B08

SFT&HW RST

Table 3-301, "Port 0 Ingress Rate Limit Control Register 2," on page 303 summerizes the PORT0_ING_RATE_CTRL2 Register 2

Table 3-301. **Port 0 Ingress Rate Limit Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_0	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_0	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_0	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	0	ING_C_UNK_UNI_RATE_EN_0	Ingress committed rate limit enable to count the unknown unticast frames
11	R/W	0	ING_C_BROAD_RATE_EN_0	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_0	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_0	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_0	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	0	ING_E_MULTI_RATE_EN_0	Ingress excess rate limit enable to count the multicast frames
6	R/W	0	ING_E_UNI_RATE_EN_0	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_0	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_0	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_0	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_0	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_0	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_0	Ingress excess rate limit enable to count the ingress mirror frames

3.7.151 PORT1_ING_RATE_CTRL0

Address 0x0B10

SFT&HW RST

Table 3-302, "Port 1 Ingress Rate Limit Control Register 0," on page 304 summerizes the PORT1_ING_RATE_CTRL0 Register 0

Table 3-302. **Port 1 Ingress Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_1	Byte number should be added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, crc and SFD.
23:22	R/W	2'b01	ING_RATE_C_TIME_SLOT_1	Committed Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
21	R/O	0	RESERVED	
20	R/W	0	ING_RATE_MODE_1	1: one two-rate three-color 0: two single rate
19:18	R/O	0	RESERVED	
17:15	R/W	0	ING_CBS_1	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_1	Committed Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.152 PORT1_ING_RATE_CTRL1

Address 0x0B14

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Table 3-303, "Port 1 Ingress Rate Limit Control Register 1," on page 304 summerizes the PORT1_ING_RATE_CTRL1 Register 1

Table 3-303. **Port 1 Ingress Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ING_BORROW_EN_1	Borrow enable
22	R/W	0	ING_RATE_UNIT_1	1: Packets/ 0: bytes
21	R/W	0	ING_CF_1	Coupling flagfor ingress rate limit
20	R/W	0	ING_CM_1	Color mode for ingress rate limit

Bit	R/W	Inital Value	Mnemonic	Description
19:18	R/W	2'b01	ING_RATE_E_TIME_SLOT_1	Excess Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
17:15	R/W	0	ING_EBS_1	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_1	Excess Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.153 PORT1_ING_RATE_CTRL2

Address 0x0B18

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Table 3-304, "Port 1 Ingress Rate Limit Control Register 2," on page 305 summerizes the PORT1_ING_RATE_CTRL2 Register 2

Table 3-304. **Port 1 Ingress Rate Limit Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	RESERVED	
15	R/W	'0	ING_C_MULTI_RATE_EN_1	Ingress committed rate limit enable to count the multicast frames
14	R/W	'0	ING_C_UNI_RATE_EN_1	Ingress committed rate limit enable to count the unicast frames
13	R/W	'0	ING_C_UNK_MULTI_RATE_EN_1	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	'0	ING_C_UNK_UNI_RATE_EN_1	Ingress committed rate limit enable to count the unknown unticast frames
11	R/W	'0	ING_C_BROAD_RATE_EN_1	Ingress committed rate limit enable to count the broadcast frames
10	R/W	'0	ING_C_MANAGE_RATE_EN_1	Ingress committed rate limit enable to count the management frames
9	R/W	'0	ING_C_TCP_CTRL_RATE_EN_1	Ingress committed rate limit enable to count the TCP control frames

Bit	R/W	Inital Value	Mnemonic	Description
8	R/W	‘0	ING_C_ING_MIRROR_RATE_EN_1	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	‘0	ING_E_MULTI_RATE_EN_1	Ingress excess rate limit enable to count the multicast frames
6	R/W	‘0	ING_E_UNI_RATE_EN_1	Ingress excess rate limit enable to count the unicast frames
5	R/W	‘0	ING_E_UNK_MULTI_RATE_EN_1	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	‘0	ING_E_UNK_UNI_RATE_EN_1	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	‘0	ING_E_BROAD_RATE_EN_1	Ingress excess rate limit enable to count the broadcast frames
2	R/W	‘0	ING_E_MANAGE_RATE_EN_1	Ingress excess rate limit enable to count the management frames
1	R/W	‘0	ING_E_TCP_CTRL_RATE_EN_1	Ingress excess rate limit enable to count the TCP control frames
0	R/W	‘0	ING_E_ING_MIRROR_RATE_EN_1	Ingress excess rate limit enable to count the ingress mirror frames

3.7.154 PORT2_ING_RATE_CTRL0

Address 0x0B20

SFT&HW RST

Table 3-305, “Port 2 Ingress Rate Limit Control Register 0,” on page 306 summerizes the PORT2_ING_RATE_CTRL0 Register 0

Table 3-305. **Port 2 Ingress Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_2	Byte number should be added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, crc and SFD.
23:22	R/W	2'b01	ING_RATE_C_TIME_SLOT_2	Committed Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
21	R/O	0	RESERVED	
20	R/W	0	ING_RATE_MODE_2	1: one two-rate three-color 0: two single rate

Bit	R/W	Inital Value	Mnemonic	Description
19:18	R/O	0	RESERVED	
17:15	R/W	0	ING_CBS_2	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_2	Committed Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.155 PORT2_ING_RATE_CTRL0

Address 0x0B24

SFT&HW RST

Table 3-306, "Port 2 Ingress Rate Limit Control Register 1," on page 307 summerizes the PORT2_ING_RATE_CTRL0 Register 1

Table 3-306. **Port 2 Ingress Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ING_BORROW_EN_2	Borrow enable
22	R/W	0	ING_RATE_UNIT_2	1: Packets/ 0: bytes
21	R/W	0	ING_CF_2	Coupling flagfor ingress rate limit
20	R/W	0	ING_CM_2	Color mode for ingress rate limit
19:18	R/W	2'b01	ING_RATE_E_TIME_SLOT_2	Excess Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
17:15	R/W	0	ING_EBS_2	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_2	Excess Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.156 PORT2_ING_RATE_CTRL2

Address 0x0B28

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Table 3-307, "Port 2 Ingress Rate Limit Control Register 2," on page 308 summerizes the PORT2_ING_RATE_CTRL2 Register 2

Table 3-307. **Port 2 Ingress Rate Limit Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_2	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_2	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_2	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	0	ING_C_UNK_UNI_RATE_EN_2	Ingress committed rate limit enable to count the unknown unticast frames
11	R/W	0	ING_C_BROAD_RATE_EN_2	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_2	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_2	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_2	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	0	ING_E_MULTI_RATE_EN_2	Ingress excess rate limit enable to count the multicast frames
6	R/W	0	ING_E_UNI_RATE_EN_2	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_2	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_2	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_2	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_2	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_2	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_2	Ingress excess rate limit enable to count the ingress mirror frames

3.7.157 PORT3_ING_RATE_CTRL0

Address 0x0B30

SFT&HW RST

Table 3-308, "Port 3 Ingress Rate Limit Control Register 0," on page 309 summerizes the PORT3_ING_RATE_CTRL0 Register 0

Table 3-308. **Port 3 Ingress Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_3	Byte number should be added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, crc and SFD.
23:22	R/W	2'b01	ING_RATE_C_TIME_SLOT_3	Committed Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
21	R/O	0	RESERVED	
20	R/W	0	ING_RATE_MODE_3	1: one two-rate three-color 0: two single rate
19:18	R/O	0	RESERVED	
17:15	R/W	0	ING_CBS_3	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_3	Committed Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.158 PORT3_ING_RATE_CTRL0

Address 0x0B34

SFT&HW RST

Table 3-309, "Port 3 Ingress Rate Limit Control Register 1," on page 310 summerizes the PORT3_ING_RATE_CTRL0 Register 1

Table 3-309. **Port 3 Ingress Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ING_BORROW_EN_3	Borrow enable
22	R/W	0	ING_RATE_UNIT_3	1: Packets/ 0: bytes
21	R/W	0	ING_CF_3	Coupling flagfor ingress rate limit
20	R/W	0	ING_CM_3	Color mode for ingress rate limit
19:18	R/W	2'b01	ING_RATE_E_TIME_SLOT_3	Excess Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
17:15	R/W	0	ING_EBS_3	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_3	Excess Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.159 PORT3_ING_RATE_CTRL2

Address 0x0B38

SFT&HW RST

Table 3-310, "Port 3 Ingress Rate Limit Control Register 2," on page 310 summerizes the PORT3_ING_RATE_CTRL2 Register 2

Table 3-310. **Port 3 Ingress Rate Limit Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_3	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_3	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_3	Ingress committed rate limit enable to count the unknown multicast frames

Bit	R/W	Inital Value	Mnemonic	Description
12	R/W	0	ING_C_UNK_UNI_RATE_EN_3	Ingress committed rate limit enable to count the unknown unticast frames
11	R/W	0	ING_C_BROAD_RATE_EN_3	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_3	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_3	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_3	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	0	ING_E_MULTI_RATE_EN_3	Ingress excess rate limit enable to count the multicast frames
6	R/W	0	ING_E_UNI_RATE_EN_3	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_3	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_3	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_3	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_3	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_3	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_3	Ingress excess rate limit enable to count the ingress mirror frames

3.7.160 PORT4_ING_RATE_CTRL0

Address 0x0B40

SFT&HW RST

Table 3-311, "Port 4 Ingress Rate Limit Control Register 0," on page 312 summerizes the PORT4_ING_RATE_CTRL0 Register 0

Table 3-311. **Port 4 Ingress Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	'h18	ADD_RATE_BYTE_4	Byte number should be added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, crc and SFD.
23:22	R/W	2'b01	ING_RATE_C_TIME_SLOT_4	Committed Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
21	R/W	0	RESERVED	
20	R/W	0	ING_RATE_MODE_4	1: one two-rate three-color 0: two single rate
19:18	R/W	0	RESERVED	
17:15	R/W	0	ING_CBS_4	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_4	Committed Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.161 PORT4_ING_RATE_CTRL0

Address 0x0B44

SFT&HW RST

Table 3-312, "Port 4 Ingress Rate Limit Control Register 1," on page 312 summerizes the PORT4_ING_RATE_CTRL0 Register 1

Table 3-312. **Port 4 Ingress Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ING_BORROW_EN_4	Borrow enable
22	R/W	0	ING_RATE_UNIT_4	1: Packets/ 0: bytes
21	R/W	0	ING_CF_4	Coupling flagfor ingress rate limit
20	R/W	0	ING_CM_4	Color mode for ingress rate limit

Bit	R/W	Inital Value	Mnemonic	Description
19:18	R/W	2'b01	ING_RATE_E_TIME_SLOT_4	Excess Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
17:15	R/W	0	ING_EBS_4	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_4	Excess Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.162 PORT4_ING_RATE_CTRL2

Address 0x0B48

SFT&HW RST

Table 3-313, "Port 4 Ingress Rate Limit Control Register 2," on page 313 summerizes the PORT4_ING_RATE_CTRL2 Register 2

Table 3-313. **Port 4 Ingress Rate Limit Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_4	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_4	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_4	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	0	ING_C_UNK_UNI_RATE_EN_4	Ingress committed rate limit enable to count the unknown unticast frames
11	R/W	0	ING_C_BROAD_RATE_EN_4	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_4	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_4	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_4	Ingress committed rate limit enable to count the ingress mirror frames

Bit	R/W	Inital Value	Mnemonic	Description
7	R/W	0	ING_E_MULTI_RATE_EN_4	Ingress excess rate limit enable to count the multicast frames
6	R/W	0	ING_E_UNI_RATE_EN_4	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_4	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_4	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_4	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_4	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_4	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_4	Ingress excess rate limit enable to count the ingress mirror frames

3.7.163 PORT5 _ING_RATE_CTRL0

Address 0x0B50

SFT&HW RST

Table 3-314, "Port 5 Ingress Rate Limit Control Register 0," on page 314 summerizes the PORT5 _ING_RATE_CTRL0 Register 0

Table 3-314. **Port 5 Ingress Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_5	Byte number should be added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, crc and SFD.
23:22	R/W	2'b01	ING_RATE_C_TIME_SLOT_5	Committed Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
21	R/O	0	RESERVED	
20	R/W	0	ING_RATE_MODE_5	1: one two-rate three-color 0: two single rate
19:18	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
17:15	R/W	0	ING_CBS_5	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_5	Committed Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.164 PORT5_ING_RATE_CTRL1

Address 0x0B54

SFT&HW RST

Table 3-315, "Port 5 Ingress Rate Limit Control Register 1," on page 315 summerizes the PORT5_ING_RATE_CTRL1 Register 1

Table 3-315. **Port 5 Ingress Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	RESERVED	
23	R/W	0	ING_BORROW_EN_5	Borrow enable
22	R/W	0	ING_RATE_UNIT_5	1: Packets/ 0: bytes
21	R/W	0	ING_CF_5	Coupling flagfor ingress rate limit
20	R/W	0	ING_CM_5	Color mode for ingress rate limit
19:18	R/W	2'b01	ING_RATE_E_TIME_SLOT_5	Excess Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
17:15	R/W	0	ING_EBS_5	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_5	Excess Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.165 PORT5_ING_RATE_CTRL2

Address 0x0B58

SFT&HW RST

Table 3-316, "Port 5 Ingress Rate Limit Control Register 2," on page 316 summerizes the PORT5_ING_RATE_CTRL2 Register 2

Table 3-316. **Port 5 Ingress Rate Limit Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_5	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_5	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_5	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	0	ING_C_UNK_UNI_RATE_EN_5	Ingress committed rate limit enable to count the unknown unticast frames
11	R/W	0	ING_C_BROAD_RATE_EN_5	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_5	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_5	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_5	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	0	ING_E_MULTI_RATE_EN_5	Ingress excess rate limit enable to count the multicast frames
6	R/W	0	ING_E_UNI_RATE_EN_5	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_5	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_5	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_5	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_5	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_5	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_5	Ingress excess rate limit enable to count the ingress mirror frames

3.7.166 PORT6 _ING_RATE_CTRL0 SFT&HW RST

Address 0x0B60

Table 3-317, "Port 6 Ingress Rate Limit Control Register 0," on page 317 summerizes the PORT6 _ING_RATE_CTRL0 Register 0

Table 3-317. **Port 6 Ingress Rate Limit Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_6	Byte number should be added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, crc and SFD.
23:22	R/W	2'b01	ING_RATE_C_TIME_SLOT_6	Committed Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
21	R/O	0	RESERVED	
20	R/W	0	ING_RATE_MODE_6	1: one two-rate three-color 0: two single rate
19:18	R/O	0	RESERVED	
17:15	R/W	0	ING_CBS_6	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_6	Committed Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.167 PORT6_ING_RATE_CTRL1

Address 0x0B64

SFT&HW RST

Table 3-318, "Port 6 Ingress Rate Limit Control Register 1," on page 318 summerizes the PORT6_ING_RATE_CTRL1 Register 1

Table 3-318. **Port 6 Ingress Rate Limit Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	'h18	RESERVED	
23	R/W	0	ING_BORROW_EN_6	Borrow enable
22	R/W	0	ING_RATE_UNIT_6	1: Packets/ 0: bytes
21	R/W	0	ING_CF_6	Coupling flagfor ingress rate limit
20	R/W	0	ING_CM_6	Color mode for ingress rate limit
19:18	R/W	2'b01	ING_RATE_E_TIME_SLOT_6	Excess Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
17:15	R/W	0	ING_EBS_6	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_6	Excess Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 15'h7FFF is for disable rate limit for ingress. if these bits are set to 15'h0, no frame should be received in from this port.

3.7.168 PORT6_ING_RATE_CTRL2

Address 0x0B68

SFT&HW RST

Table 3-319, "Port 6 Ingress Rate Limit Control Register 2," on page 318 summerizes the PORT6_ING_RATE_CTRL2 Register 2

Table 3-319. **Port 6 Ingress Rate Limit Control Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_6	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_6	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_6	Ingress committed rate limit enable to count the unknown multicast frames

Bit	R/W	Inital Value	Mnemonic	Description
12	R/W	0	ING_C_UNK_UNI_RATE_EN_6	Ingress committed rate limit enable to count the unknown unticast frames
11	R/W	0	ING_C_BROAD_RATE_EN_6	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_6	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_6	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_6	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	0	ING_E_MULTI_RATE_EN_6	Ingress excess rate limit enable to count the multicast frames
6	R/W	0	ING_E_UNI_RATE_EN_6	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_6	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_6	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_6	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_6	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_6	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_6	Ingress excess rate limit enable to count the ingress mirror frames

3.7.169 CPU_GROUP_CTRL

Address 0x0B70

SFT&HW RST

Table 3-320, "To CPU Packet Remap Priority Control Register," on page 319 summerizes the CPU_GROUP_CTRL Register

Table 3-320. **To CPU Packet Remap Priority Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	CPU_GROUP_REMAP_EN	Remap the packet(to CPU) priority
30:23	R/O	0	RESERVED	
22:20	R/W	0	CPU_GROUP5_PRI	Header type5'h19~5'h1A
19	R/O	0	RESERVED	

Bit	R/W	Inital Value	Mnemonic	Description
18:16	R/W	1	CPU_GROUP4_PRI	Header type5'h17~5'h18
15	R/O	0	RESERVED	
14:12	R/W	2	CPU_GROUP3_PRI	Header type5'hE~5'h16
11	R/O	0	RESERVED	
10:8	R/W	3	CPU_GROUP2_PRI	Header type5'h5~5'hD
7	R/O	0	RESERVED	
6:4	R/W	4	CPU_GROUP1_PRI	Header type 5'h3,5'h4
3	R/O	0	RESERVED	
2:0	R/W	5	CPU_GROUP0_PRI	Header type5'h1,5'h2.5'h1C

3.8 PKT EDIT REGISTER(Address Range 0x0C00 ~ 0x0C64)

Table 3-321 summarizes the Packet Editor registers.

Table 3-321. **Packet Editor Register Summary**

Name	Address	Reset
PKT EDIT CONTROL REGISTER	0x0C00	HARD & SOFT
PORT0 QUEUE REMAP REGISTER	0x0C40~0x0C44	HARD & SOFT
PORT1 QUEUE REMAP REGISTER	0x0C48	HARD & SOFT
PORT2 QUEUE REMAP REGISTER	0x0C4C	HARD & SOFT
PORT3 QUEUE REMAP REGISTER	0x0C50	HARD & SOFT
PORT4 QUEUE REMAP REGISTER	0x0C54	HARD & SOFT
PORT5 QUEUE REMAP REGISTER	0x0C58~0x0C5C	HARD & SOFT
PORT6 QUEUE REMAP REGISTER	0x0C60~0x0C64	HARD & SOFT

3.8.1 PKT_EDIT_CTRL

Address 0x0C00

SFT&HW RST

Table 3-322, "PKT Edit Control Register PORT0_QUEUE_REMAP_REG0," on page 321 summerizes the PKT_EDIT_CTRL Register

Table 3-322. **PKT Edit Control Register PORT0_QUEUE_REMAP_REG0**

Bit	R/W	Inital Value	Mnemonic	Description
31:27	R/O	0	RESERVED	
26	R/W	0	VLAN_PRI_REMAP_EN_6	1'b1: frame send out from port6, should remap priority based on frame priority.
25	R/W	0	VLAN_PRI_REMAP_EN_5	1'b1: frame send out from port5, should remap priority based on frame priority.
24	R/W	0	VLAN_PRI_REMAP_EN_4	1'b1: frame send out from port4, should remap priority based on frame priority.
23	R/W	0	VLAN_PRI_REMAP_EN_3	1'b1: frame send out from port3, should remap priority based on frame priority.
22	R/W	0	VLAN_PRI_REMAP_EN_2	1'b1: frame send out from port2, should remap priority based on frame priority.
21	R/W	0	VLAN_PRI_REMAP_EN_1	1'b1: frame send out from port1, should remap priority based on frame priority.
20	R/W	0	VLAN_PRI_REMAP_EN_0	1'b1: frame send out from port0, should remap priority based on frame priority.
19:12	R/W	0	IP_TTL	
11	R/W	0	IP_TTL_CHANGE_EN	1'b1: frame TTL change to IP_TTL.

Bit	R/W	Inital Value	Mnemonic	Description
10	R/W	0	IPV4_ID_RANDOM_EN	1'b1: frame should send out with random ID.
9	R/W	0	IPV4_DF_CLEAR_EN	1'b1: ipv4 DF field cleared to zero
8	R/O	0	RESERVED	
7	R/O	0	RESERVED	
6:0	R/O	0	RESERVED	

Address 0x0C40

SFT&HW RST

Table 3-323, "Port 0 Queue Remap Register Register," on page 322 summerizes the PORT0_QUEUE_REMAP_REG0 Register

Table 3-323. **Port 0 Queue Remap Register Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	PORT0_QUEUE3_EN	Enable queue 3 remap
30:28	R/O	0	RESERVED	
27:24	R/W	0	PORT0_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT0_QUEUE2_EN	Enable queue 2 remap
22:20	R/O	0	RESERVED	
19:16	R/W	0	PORT0_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT0_QUEUE1_EN	Enable queue 1 remap
14:12	R/O	0	RESERVED	
11:8	R/W	0	PORT0_QUEUE1_IDX	Queue 1 remap table index
7	R/W	0	PORT0_QUEUE0_EN	Enable queue 0 remap
6:4	R/O	0	RESERVED	
3:0	R/W	0	PORT0_QUEUE0_IDX	Queue 0 remap table index

3.8.2 PORT0_QUEUE_REMAP_REG1

Address 0x0C44

SFT&HW RST

Table 3-324, "Port 0 Queue Remap Register Register 1," on page 323 summerizes the PORT0_QUEUE_REMAP_REG1 Register 1

Table 3-324. **Port 0 Queue Remap Register Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	RESERVED	
15	R/W	0	PORT0_QUEUE5_EN	Enable queue 5 remap
14:12	R/O	0	RESERVED	
11:8	R/W	0	PORT0_QUEUE5_IDX	Queue 5 remap table index
7	R/W	0	PORT0_QUEUE4_EN	Enable queue 4 remap
6:4	R/O	0	RESERVED	
3:0	R/W	0	PORT0_QUEUE4_IDX	Queue 4 remap table index

3.8.3 PORT1_QUEUE_REMAP_REG0

Address 0x0C48

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Table 3-325, "Port 1 Queue Remap Register Register 0," on page 323 summerizes the PORT1_QUEUE_REMAP_REG0 Register 0

Table 3-325. **Port 1 Queue Remap Register Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	PORT1_QUEUE3_EN	Enable queue 3 remap
30:28	R/O	0	RESERVED	
27:24	R/W	0	PORT1_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT1_QUEUE2_EN	Enable queue 2 remap
22:20	R/O	0	RESERVED	
19:16	R/W	0	PORT1_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT1_QUEUE1_EN	Enable queue 1 remap
14:12	R/O	0	RESERVED	
11:8	R/W	0	PORT1_QUEUE1_IDX	Queue 1 remap table index
7	R/W	0	PORT1_QUEUE0_EN	Enable queue 0 remap
6:4	R/O	0	RESERVED	
3:0	R/W	0	PORT1_QUEUE0_IDX	Queue 0 remap table index

3.8.4 PORT2_QUEUE_REMAP_REG0

Address 0x0C4C

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Table 3-326, "Port 2 Queue Remap Register Register," on page 324 summerizes the PORT2_QUEUE_REMAP_REG0 Register

Table 3-326. **Port 2 Queue Remap Register Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	PORT2_QUEUE3_EN	Enable queue 3 remap
30:28	R/O	0	RESERVED	
27:24	R/W	0	PORT2_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT2_QUEUE2_EN	Enable queue 2 remap
22:20	R/O	0	RESERVED	
19:16	R/W	0	PORT2_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT2_QUEUE1_EN	Enable queue 1 remap
14:12	R/O	0	RESERVED	
11:8	R/W	0	PORT2_QUEUE1_IDX	Queue 1 remap table index
7	R/W	0	PORT2_QUEUE0_EN	Enable queue 0 remap
6:4	R/O	0	RESERVED	
3:0	R/W	0	PORT2_QUEUE0_IDX	Queue 0 remap table index

3.8.5 PORT3_QUEUE_REMAP_REG0

Address 0x0C50

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Table 3-327, "Port 3 Queue Remap Register Register 0," on page 324 summerizes the PORT3_QUEUE_REMAP_REG0 Register 0

Table 3-327. **Port 3 Queue Remap Register Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	PORT3_QUEUE3_EN	Enable queue 3 remap
30:28	R/O	0	RESERVED	
27:24	R/W	0	PORT3_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT3_QUEUE2_EN	Enable queue 2 remap
22:20	R/O	0	RESERVED	
19:16	R/W	0	PORT3_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT3_QUEUE1_EN	Enable queue 1 remap
14:12	R/O	0	RESERVED	
11:8	R/W	0	PORT3_QUEUE1_IDX	Queue 1 remap table index

Bit	R/W	Inital Value	Mnemonic	Description
7	R/W	0	PORT3_QUEUE0_EN	Enable queue 0 remap
6:4	R/O	0	RESERVED	
3:0	R/W	0	PORT3_QUEUE0_IDX	Queue 0 remap table index

3.8.6 PORT4_QUEUE_REMAP_REG0

Address 0x0C54

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Table 3-328, "Port 4 Queue Remap Register Register 0," on page 325 summerizes the PORT4_QUEUE_REMAP_REG0 Register 0

Table 3-328. **Port 4 Queue Remap Register Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	PORT4_QUEUE3_EN	Enable queue 3 remap
30:28	R/O	0	RESERVED	
27:24	R/W	0	PORT4_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT4_QUEUE2_EN	Enable queue 2 remap
22:20	R/O	0	RESERVED	
19:16	R/W	0	PORT4_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT4_QUEUE1_EN	Enable queue 1 remap
14:12	R/O	0	RESERVED	
11:8	R/W	0	PORT4_QUEUE1_IDX	Queue 1 remap table index
7	R/W	0	PORT4_QUEUE0_EN	Enable queue 0 remap
6:4	R/O	0	RESERVED	
3:0	R/W	0	PORT4_QUEUE0_IDX	Queue 0 remap table index

3.8.7 PORT5_QUEUE_REMAP_REG0

Address 0x0C58

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Table 3-329, "Port 5 Queue Remap Register Register 0," on page 326 summerizes the PORT5_QUEUE_REMAP_REG0 Register 0

Table 3-329. **Port 5 Queue Remap Register Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	PORT5_QUEUE3_EN	Enable queue 3 remap
30:28	R/O	0	RESERVED	
27:24	R/W	0	PORT5_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT5_QUEUE2_EN	Enable queue 2 remap
22:20	R/O	0	RESERVED	
19:16	R/W	0	PORT5_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT5_QUEUE1_EN	Enable queue 1 remap
14:12	R/O	0	RESERVED	
11:8	R/W	0	PORT5_QUEUE1_IDX	Queue 1 remap table index
7	R/W	0	PORT5_QUEUE0_EN	Enable queue 0 remap
6:4	R/O	0	RESERVED	
3:0	R/W	0	PORT5_QUEUE0_IDX	Queue 0 remap table index

3.8.8 PORT5_QUEUE_REMAP_REG1

Address 0x0C5C

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Table 3-330, "Port 5 Queue Remap Register Register 1," on page 326 summerizes the **PORT5_QUEUE_REMAP_REG1** Register 1

Table 3-330. **Port 5 Queue Remap Register Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	RESERVED	
15	R/W	0	PORT5_QUEUE5_EN	Enable queue 5 remap
14:12	R/O	0	RESERVED	
11:8	R/W	0	PORT5_QUEUE5_IDX	Queue 5 remap table index
7	R/W	0	PORT5_QUEUE4_EN	Enable queue 4 remap
6:4	R/O	0	RESERVED	
3:0	R/W	0	PORT5_QUEUE4_IDX	Queue 4 remap table index

3.8.9 PORT6_QUEUE_REMAP_REG0

Address 0x0C60

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Table 3-331, "Port 6 Queue Remap Register Register," on page 327 summerizes the PORT6_QUEUE_REMAP_REG0 Register

Table 3-331. **Port 6 Queue Remap Register Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	PORT6_QUEUE3_EN	Enable queue 3 remap
30:28	R/O	0	RESERVED	
27:24	R/W	0	PORT6_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT6_QUEUE2_EN	Enable queue 2 remap
22:20	R/O	0	RESERVED	
19:16	R/W	0	PORT6_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT6_QUEUE1_EN	Enable queue 1 remap
14:12	R/O	0	RESERVED	
11:8	R/W	0	PORT6_QUEUE1_IDX	Queue 1 remap table index Enable queue 0 remap Queue 0 remap table index
7	R/W	0	PORT6_QUEUE0_EN	Enable queue 0 remap
6:4	R/O	0	RESERVED	
3:0	R/W	0	PORT6_QUEUE0_IDX	Queue 0 remap table index

3.8.10 PORT6_QUEUE_REMAP_REG0

Address 0x0C64

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Table 3-332, "Port 6 Queue Remap Register Register 1," on page 327 summerizes the PORT6_QUEUE_REMAP_REG0 Register 1

Table 3-332. **Port 6 Queue Remap Register Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/0	0	RESERVED	
15	R/W	0	PORT6_QUEUE5_EN	Enable queue 5 remap
14:12	R/O	0	RESERVED	
11:8	R/W	0	PORT6_QUEUE5_IDX	Queue 5 remap table index
7	R/O	0	PORT6_QUEUE4_EN	Enable queue 4 remap
6:4	R/O	0	RESERVED	
3:0	R/W	0	PORT6_QUEUE4_IDX	Queue 4 remap table index

3.8.11 Router Default VID Register 0

Address: 0x0C70

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Table 3-333 summerizes the router default VID register 0.

Table 3-333. **Router Default VID Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	Reserved	
27:16	R/W	1	ROUTER_DEFAULT_VID1	Port 1 default VID for router
15:12	R/O	0	Reserved	
11:0	R/W	1	ROUTER_DEFAULT_VID0	Port 0 default VID for router

3.8.12 Router Default VID Register 1

Address: 0x0C74

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Table 3-334 summerizes the router default VID register 1.

Table 3-334. **Router Default VID Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	Reserved	
27:16	R/W	1	ROUTER_DEFAULT_VID3	Port 3 default VID for router
15:12	R/O	0	Reserved	
11:0	R/W	1	ROUTER_DEFAULT_VID2	Port 2 default VID for router

3.8.13 Router Default VID Register 2

Address: 0x0C78

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Table 3-335 summerizes the router default VID register 2.

Table 3-335. **Router Default VID Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0	Reserved	
27:16	R/W	1	ROUTER_DEFAULT_VID5	Port 5 default VID for router
15:12	R/O	0	Reserved	
11:0	R/W	1	ROUTER_DEFAULT_VID4	Port 4 default VID for router

3.8.14 Router Default VID Register 3

Address: 0x0C7C

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Table 3-336 summerizes the router default VID register 3.

Table 3-336. **Router Default VID Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:12	R/O	0	Reserved	
11:0	R/W	1	ROUTER_DEFAULT_VID6	Port 6 default VID for router

3.8.15 Router Egress VLAN Mode

Address: 0x0C80

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Table 3-337 summerizes the router default VID register 3.

Table 3-337. **Router Default VID Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:26	R/O	0	Reserved	
25:24	R/W	0	ROUTER_EG_VLAN_MODE6	Router egress VLAN mode of port 6
23:22	R/O	0	Reserved	
21:20	R/W	0	ROUTER_EG_VLAN_MODE5	Router egress VLAN mode of port 5
19:18	R/O	0	Reserved	
17:16	R/W	0	ROUTER_EG_VLAN_MODE4	Router egress VLAN mode of port 4
15:14	R/O	0	Reserved	
13:12	R/W	0	ROUTER_EG_VLAN_MODE3	Router egress VLAN mode of port 3
11:10	R/O	0	Reserved	
9:8	R/W	0	ROUTER_EG_VLAN_MODE2	Router egress VLAN mode of port 2
7:6	R/O	0	Reserved	
5:4	R/W	0	ROUTER_EG_VLAN_MODE1	Router egress VLAN mode of port 1
3:2	R/O	0	Reserved	
1:0	R/W	0	ROUTER_EG_VLAN_MODE0	Router egress VLAN mode of port 0 00 = Egress transmits frames unmodified 01 = Egress transmits frames without VLAN 10 = Egress transmits frames with VLAN 11 = Untouched

3.9 L3 REGISTER (Address Range 0x0E00 ~ 0x0E5C)

Table 3-338, "L3 Register Summary," on page 330 summarizes the *L3 REGISTER* registers.

Table 3-338. **L3 Register Summary**

Name	Address	Reset
HROUTER CONTROL REGISTER	0x0E00	HARD & SOFT
HROUTER PORT BASED CONTROL REGISTER	0x0E04~0x0E0C	HARD & SOFT
WCMP HASH TABLE REGISTER	0x0E10~0x0E1C	HARD & SOFT
WCMP NEXT HOP TABLE REGISTER	0x0E20~0x0E2C	HARD & SOFT
ARP ENTRY LOCK CONTROL REGISTER	0x0E30	HARD & SOFT
ARP USED ACCOUNT REGISTER	0x0E34	HARD & SOFT
HNAT CONTROL REGISTER	0x0E38	HARD & SOFT
NAPT ENTRY LOCK CONTROLREGISTER	0x0E3C~0x0E40	HARD & SOFT
NAPT USED ACCOUNT REGISTER	0x0E44	HARD & SOFT
ENTRY EDIT DATA REGISTER	0x0E48~0x0E54	HARD & SOFT
ENTRY EDIT CONTROL REGISTER	0x0E58	HARD & SOFT
PRIVATE BASE IP ADDR REGISTER	0x0E5C	HARD & SOFT

3.9.1 HRouter_control

Address 0x0E00

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Table 3-339, "HRouter Register," on page 330 summerizes the HRouter_control Register

Table 3-339. **HRouter Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:20	R/O	0	RESERVED	
19	R/W	0	ARP_LEARN_MODE	1: Learn All ARP 0: Only learn ARP to Router.
18	R/W	0x1	ARP_OVERWRITE_EN	1: overwrite enable
17:16	R/W	0x3	GLOBAL_LOCK_TIME	0:Disable 1:100us 2:1ms 3:10ms When edit one entry, should lock current entry for a period; For example overwrite session when auto learn, or cpu force to write one session
15:8	R/W	0x24	ARP_AGE_TIME	6s*N, 0: ARP Aging Disable

Bit	R/W	Inital Value	Mnemonic	Description
7:4			WCMP_HASH_EN	WCMP hash key support one or more field from SIP/SP/DIP/DP, every field has individual control bit to enable/ disable it; Bit0: SIP Bit1: SP Bit2: DIP Bit3: DP 1: enable 0: disable
3:2	R/W	0	RESERVED	
1	R/O	0	ARP_AGE_MODE	0: normal age mode; 1:stop age when age_flagis 1;
0	R/W	0x1	ROUTER_EN	1: To enable Host routing 0: Disable Host routing

3.9.2 HRouter_Pbased_Control0

Address 0x0E04

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Table 3-340, "Router Port Based Control Register 0," on page 331 summerizes the HRouter_Pbased_Control0 Register 0

Table 3-340. **Router Port Based Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:21	R/O	0	RESERVED	
20:0	R/W	0	ARP_SOURCE_CHECK_MODE	Source check Mode for ARP 0: Disable 1: Check SMAC & SIP 2: Check SMAC & SIP & SP 3. Check SMAC & SIP & VID 4. Check SMAC & SIP & SP & VID Port Based Control Bit 2:0 for port 0 Bit 5:3 for port 1 ……

3.9.3 HRouter_Pbased_Control1

Address 0x0E08

SFT&HD RST

Table 3-341, "HRouter Port Based Control Register 1," on page 332 summerizes the HRouter_Pbased_Control1 Register 1

Table 3-341. **HRouter Port Based Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:21	R/O	0	RESERVED	
20:0	R/W	0	IP_SOURCE_CHECK_MODE	Source check mode for normal packet 0: Disable 1: Check SMAC & SIP 2: Check SMAC & SIP & SP 3. Check SMAC & SIP & VID 4. Check SMAC & SIP & SP & VID Port Based Control Bit 2:0 for port 0 Bit 5:3 for port 1 ……

3.9.4 HRouter_Pbased_Control2

Address 0x0E0C

SFT&HD RST

Table 3-342, "HRouter Port Based Control 2 Register 2," on page 332 summerizes the HRouter_Pbased_Control2 Register 2

Table 3-342. **HRouter Port Based Control 2 Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:23	R/O	0	RESERVED	
22:16	R/W	0x7f	IP_SP_UPDATE_EN	Source Port Update enable Can update only when IP+MAC+VID match arp entry and no source check violation; Port Based Control Bit 16: for port 0 Bit 17: for port 1 ….
15	RO	0	RESERVED	
14:8	R/W	0	ARP_REP_LEARN_EN	ARP reply learn enable Port Based Control Bit 8: for port 0 Bit 9: for port 1…….

Bit	R/W	Inital Value	Mnemonic	Description
7	RO	0	RESERVED	
6:0	R/W	0	ARP_REQ_LEARN_EN	ARP request learn enable Port Based Control Bit 0: for port 0 Bit 1: for port 1

3.9.5 WCMP_HASH_TABLE0

Address 0x0E10

SFT&HD RST

Table 3-343, "WCMP Hash Table 0 Register," on page 333 summerizes the WCMP_HASH_TABLE0 Register

Table 3-343. **WCMP Hash Table 0 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W	0	WCMP_HASH_TABLE0	

3.9.6 WCMP_HASH_TABLE1

Address 0x0E14

SFT&HD RST

Table 3-344, "WCMP Hash Table 1 Register," on page 333 summerizes the WCMP_HASH_TABLE1 Register

Table 3-344. **WCMP Hash Table 1 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W	0	WCMP_HASH_TABLE1	

3.9.7 WCMP_HASH_TABLE2

Address 0x0E18

SFT&HD RST

Table 3-345, "WCMP Hash Table 2 Register," on page 334 summerizes the WCMP_HASH_TABLE2 Register

Table 3-345. **WCMP Hash Table 2 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W	0	WCMP_HASH_TABLE2	

3.9.8 WCMP_HASH_TABLE3

Address 0x0E1C

SFT&HD RST

Table 3-346, "WCMP Hash Table 3 Register," on page 334 summerizes the WCMP_HASH_TABLE3 Register

Table 3-346. **WCMP Hash Table 3 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W	0	WCMP_HASH_TABLE3	

3.9.9 WCMP_NHOP_TABLE0

Address 0x0E20

SFT&HD RST

Table 3-347, "WCMP Next Hop Table 0 Register," on page 334 summerizes the WCMP_NHOP_TABLE0 Register

Table 3-347. **WCMP Next Hop Table 0 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W	0	WCMP_NHOP_TABLE0	Bit7: Next Hop0 valid Bit6:0: Next Hop0 index Next hop1~3 use the same rule; Every next hop use 8 bit, total 4 next hops for every 32 bits;

3.9.10 WCMP_NHOP_TABLE1

Address 0x0E24

SFT&HD RST

Table 3-348, "WCMP Next Hop Table 1 Register," on page 335 summerizes the WCMP_NHOP_TABLE1 Register

Table 3-348. **WCMP Next Hop Table 1 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W	0	WCMP_NHOP_TABLE1	Bit7: Next Hop0 valid Bit6:0: Next Hop0 index Next hop1~3 use the same rule; Every next hop use 8 bit, total 4 next hops for every 32 bits;

3.9.11 WCMP_NHOP_TABLE2

Address 0x0E28

SFT&HD RST

Table 3-349, "WCMP Next Hop Table 2 Register," on page 335 summerizes the WCMP_NHOP_TABLE2 Register

Table 3-349. **WCMP Next Hop Table 2 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W	0	WCMP_NHOP_TABLE2	Bit7: Next Hop0 valid Bit6:0: Next Hop0 index Next hop1~3 use the same rule; Every next hop use 8 bit, total 4 next hops for every 32 bits;

3.9.12 WCMP_NHOP_TABLE3

Address 0x0E2C

SFT&HD RST

Table 3-350, "WCMP Next Hop Table 3 Register," on page 335 summerizes the WCMP_NHOP_TABLE3 Register

Table 3-350. **WCMP Next Hop Table 3 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W	0	WCMP_NHOP_TABLE3	Bit7: Next Hop0 valid Bit6:0: Next Hop0 index Next hop1~3 use the same rule; Every next hop use 8 bit, total 4 next hops for every 32 bits;

3.9.13 ARP_Entry_Lock_Control

Address 0x0E30

SFT&HD RST

Table 3-351, "ARP Entry Lock Control Register," on page 336 summerizes the ARP_Entry_Lock_Control Register

Table 3-351. **ARP Entry Lock Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	ARP_SW_LOCK_EN	When enabled, specific entry always locked by software; When disabled, lock_index show locked entry by hardware itself.
30:11	R/O	0	RESERVED	
10	R/O	0	ARP_HW_LOCK_STATUS	When software lock disable, the HW_lock_status shows the lock status by hardware;
9:7	R/O	0	RESERVED	
6:0	R/W	0	ARP_LOCK_INDEX	DEPEND:arp_hw_lock_en, arp_hw_lock_index[6:0], Entry index locked by software or hardware;

3.9.14 ARP_Used_Account

Address 0x0E34

SFT&HD RST

Table 3-352, "ARP Used Account Register," on page 336 summerizes the ARP_Used_Account Register

Table 3-352. **ARP Used Account Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:8	R/O	0	RESERVED	
7:0	R/O	0	ARP_USED_CNT	Total used session in ARP table;

3.9.15 HNAT_Control

Address 0x0E38

SFT&HD RST

Table 3-353, "HNAT Control Register," on page 337 summerizes the HNAT_Control Register

Table 3-353. **HNAT Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:23	R/O	0	RESERVED	
22	R/W	0	NAPT_AGE_SPD_UP_STEP	0:Double 1:Quadruple To control the speed up degree, if set as 0, double the aging speed, if set as 1,quadruple the aging speed;
21:20	R/W	2	NAPT_AGE_SPD_UP_THRESH	0:Disable; 1:1/4; 2:1/8, 3:1/16 The ratio of the remaining entry number; when reach the ratio, aging scheme will speed up
19:18	R/W	0	NAPT_UDP_AGE_STEP	0:1 1:2 2:3 3:4 To set the UDP aging step value
17:16	R/W	0	NAPT_TCP_AGE_STEP	0:1 1:2 2:3 3:4 To set the TCP aging step value,GRE share the same setting;
15:8	R/W	0xa	NAPT_AGE_TIMER	28sxN N=0, Aging Disable NAPT and GRE share the same age setting
7	R/W	0	NAPT_AGE_MODE	0:normal age mode; 1:stop age when napt age_flag is 1;
6:5	R/W	2	NAT_HASH_MODE	0: SP 1: SIP 2: SP+SIP 3: Reserved
4	R/W	1	NAPT_OVERWRITE_EN	1: when entry violation, new entry can overwrite old entry; 0: Cannot overwrite;
3:2	R/W	0	NAPT_MODE	0: Full Cone Mode 1: Strict Cone Mode 2: Port strict mode/Symmetric Mode 3: Reserved
1	R/W	1	HNAT_EN	Enable or Disable Basic NAT
0	R/W	1	HNAPT_EN	Enable or Disable HNAPT

3.9.16 NAPT_Entry_Lock_Control0 SFT&HD RST

Address 0x0E3C

Table 3-354, "NAPT Entry Lock Control Register 0," on page 338 summerizes the NAPT_Entry_Lock_Control0 Register 0

Table 3-354. **NAPT Entry Lock Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	NAPT_SW_LOCK_EN0	When enabled, specific entry always locked by software; When disabled, lock_index show locked entry by hardware itself.
30:11	R/O	0	RESERVED	
10	R/O	0	NAPT_HW_LOCK_STATUS0	When software lock disable, the HW_lock_status shows the lock status by hardware;
9:0	R/WW	0	NAPT_LOCK_INDEX0	DEPEND: napt_hw_lock_en0,napt_hw_lock_index0[9:0], Entry index locked by software or hardware;

3.9.17 NAPT_Entry_Lock_Control1

Address 0x0E40

SFT&HD RST

Table 3-355, "NAPT Entry Lock Control Register 1," on page 338 summerizes the NAPT_Entry_Lock_Control1Register

Table 3-355. **NAPT Entry Lock Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	NAPT_SW_LOCK_EN1	When enabled, specific entry always locked by software; When disabled, lock_index show locked entry by hardware itself.
30:11	R/O	0	RESERVED	
10	R/O	0	NAPT_HW_LOCK_STATUS1	When software lock disable, the HW_lock_status shows the lock status by hardware;
9:0	R/WW	0	NAPT_LOCK_INDEX1	DEPEND: napt_hw_lock_en1,napt_hw_lock_index1[9:0], Entry index locked by software or hardware;

3.9.18 NAPT_Used_Account

Address 0x0E44

SFT&HD RST

Table 3-356, "NAPT Used Account Register," on page 339 summerizes the NAPT_Used_Account Register

Table 3-356. **NAPT Used Account Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:11	R/O	0	RESERVED	
10:0	R/O	0	NAPT_USED_CNT	Total used session in NAPT table;

3.9.19 Entry_Edit_Data0

Address 0x0E48

SFT&HD RST

Table 3-357, "Entry Edit Data 0 Register," on page 339 summarizes the Entry_Edit_Data0 Register

Table 3-357. **Entry Edit Data 0 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W W	0	ENTRY_EDIT_DATA0	DEPEND:cmd_complete,entry_data0_in[31:0],

3.9.20 Entry_Edit_Data1

Address 0x0E4C

SFT&HD RST

Table 3-358, "Entry Edit Data 1 Register," on page 339 summarizes the Entry_Edit_Data1 Register

Table 3-358. **Entry Edit Data 1 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W W	0	ENTRY_EDIT_DATA1	DEPEND:cmd_complete,entry_data1_in[31:0],

3.9.21 Entry_Edit_Data2

SFT&HD RST

Address 0x0E50

Table 3-359, "Entry Edit Data 2 Register," on page 340 summarizes the Entry_Edit_Data2 Register

Table 3-359. **Entry Edit Data 2 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W W	0	ENTRY_EDIT_DATA2	DEPEND:cmd_complete,entry_data2_in[31:0],

3.9.22 Entry_Edit_Data3

Address 0x0E54

SFT&HD RST

Table 3-360, "Entry Edit Data 3 Register," on page 340 summarizes the Entry_Edit_Data3 Register

Table 3-360. **Entry Edit Data 3 Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:0	R/W W	0	ENTRY_EDIT_DATA3	DEPEND:cmd_complete,entry_data3_in[31:0],

3.9.23 Entry_Edit_control

Address 0x0E58

SFT&HD RST

Table 3-361, "Entry Edit Control Register," on page 340 summarizes the *Entry_Edit_control* Register

Table 3-361. **Entry Edit Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/WSC	0	BUSY	DEPEND:cmd_complete, 1: Write 1 to start operation; 0: HW clear to indicate operation complete
30:23	R/O	0	RESERVE	
22	R/W	0	SPECIFIC_SP_EN	Enable specific source port for flush and get next command, valid for ARP table;
21	R/W	0	SPECIFIC_VID	Enable specific VID for flush and get next command, valid for ARP table;

Bit	R/W	Inital Value	Mnemonic	Description
20	R/W	0	SPECIFIC_PIP_EN	Enable specific public ip for flush and get next command, valid for NAPT table; If enabled, according tip index field should be fill in for the command;
19	R/W	0	SPECIFIC_SIP_EN	Enable specific source ip for flush and get next command, valid for NAPT table;
18	R/W	0	SPECIFIC_AGE_EN	Enable specific age value for flush and get next command, valid for NAPT and ARP table; Use <= as compare way(and >0 is the implied condition)
17	R/WW	0	CMD_INDEX	DEPEND:cmd_complete, cmd_index_in[9:0], a. For NAT table, should fill in index for add one/delete one/search one command; b. For NAPT and ARP table, should fill in index for get next command; For example, if fill in 0, search from 1, and so on, for napt table , if fill in 1023, should search from 0, for arp table , if fill in 127 , also should search from 0; c. For NAPT and ARP table, hardware will return entry index information for ADD ONE/DELETE ONE/ SEARCH ONE command;
7:8	R/O	0	STATUS	DEPEND: cmd_complete,
6	R/O	0	RESERVED	
5:4	R/W	0	TABLE_SEL	0:NAPT Table 1:Reserved 2:NAT Table 3:ARP Table
3	R/O	0	RESERVED	
2:0	R/W	0	ENTRY_FUNC	0: No Action 1: Flush Entry 2: Add one Entry 3: Delete one Entry 4: Get Next Valid Entry, Not Valid for SIP table and NAT Table, 5: Search one Entry a.. For NAPT and ARP table, should fill in key for add one/delete one /search one;Should fill in the 5-tupe as search key(Private IP, Private Port Number, Public IP Public Port number, Protocol),for GRE entry (Private IP, Call ID, Public IP, Call ID, Protocol), for ARP table, should fill in Destination IP as search key; b. For Flush and get next command if need extra condition, should fill in related content to according field which defined in entry data structure, and set according enable control bit define in bits18~bit22;

3.9.24 Private_Base_IP_ADDR Register

Address 0x0E5C

SFT&HD RST)

Table 3-362, "Private Base IP ADDR Register," on page 342 summarizes the Private_Base_IP_ADDR Register

Table 3-362. **Private Base IP ADDR Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:20	R/O	0	RESERVED	
19:0	R/W	20'hC0A80	PRIVATE_BASE_IP_ADDR	To form 32 private ip address with low 12 IP address in NAPT table

3.10 PHY Control Registers

Table 3-363, "PHY Control Register Summary," on page 343 summarizes the PHY Control register

Table 3-363. **PHY Control Register Summary**

Offset (Hex)	Description	Page
0	Control Register	
1	Status Register	
2	PHY Identifier	
3	PHY Identifier 2	
4	Auto-negotiation Advertisement Register	
5	Link Partner Ability Register	
6	Auto-negotiation Expansion Register	
7	Next Page Transmit Register	
8	Link Partner Next Page Register	
9	1000Base-T Control Register	
A	1000Base-T Status Register	
B	Reserved	
C	Reserved	
D	Reserved	
E	Reserved	
F	Extended Status Register	
10	PHY-specific Control Register	
11	PHY-specific Status Register	
12	Interrupt Enable Register	
13	Interrupt Status Register	
14	Extended PHY-specific Register	
15	Receive Error Counter Register	
16	Virtual Cable Tester Control Register	
17	Reserved	
18	Reserved	
19	Reserved	
1A	Reserved	
1B	Reserved	
1C	Virtual Cable Tester Status Register	
1D	Debug port 1 (Address Offset)	
1E	Debug port 2 (Data Port)	
1F	Reserved	

Table 3-364, "PHY Control Register Summary — MMD3," on page 344 summarizes the PHY Control

register

Table 3-364. **PHY Control Register Summary — MMD3**

Offset (Hex)	Description	Page
0	PCS Control Register	
1	PCS Status Register	
E	EEE Capability	
16	EEE Wake Error Counter	

NOTE: The table above gives a summary of the registers in MMD7 (MDIO Managable Device address 7 for PCS)

Table 3-365, "PHY Control Register Summary — MMD7," on page 344 summarizes the PHY Control register

Table 3-365. **PHY Control Register Summary — MMD7**

Offset	Description	Page
0	AN Control	
1	AN Status	
5	AN Package Register	
2	AN XNP Transmit	
17	ANXNP Transmit1	
18	ANXNP Transmit2	
19	ANXNP Ability	
1A	ANXNP Ability1	
1B	ANXNP Ability2	
3C	EEE Advertisement	
3D	EEE LP Advertisement	
8000	EEE Ability Auto-negotiation Result	

NOTE: The table above gives a summary of the registers in MMD7 (MDIO Managable Device address 7 for PCS)

3.10.1 Control Register

Address Offset: 0x00

Table 3-366, "Control Register," on page 345 summarizes the Register

Table 3-366. **Control Register**

Bit	Symbol	Type		Description
15	Reset	Mode	R/W	PHY Software Reset. Writing a "1" to this bit causes the PHY the reset operation is done , this bit is cleared to "0" automatically. The reset occurs immediately. 1= PHY reset 0 =Normal operation
		HW Rst	0	
		SW Rst	SC	
14	Loopback	Mode	R/W	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. 1 = Enable Loopback 0 = Disable Loopback
		HW Rst	0	
		SW Rst	0	
13	Speed Selection	Mode	R/W	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1= 100 Mb/s 0 0 = 10 Mb/s
		HW Rst		
		SW Rst		
12	Auto-negotiation	Mode	R/W	1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
		HW Rst		
		SW Rst		
11	Power Down	Mode	R/W	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0.9) are not set by the user. 1 = Power down 0 = Normal operation
		HW Rst	0	
		SW Rst	0	
10	Isolate	Mode	R/W	The GMII/MII output pins are tristated when this bit is set to 1. The GMII/MII inputs are ignored. 1 = Isolate 0 = Normal operation
		HW Rst	0	
		SW Rst	0	
9	Restart Auto-negotiation	Mode	R/W, SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
		HW Rst	0	
		SW Rst	SC	
8	Duplex Mode	Mode	R/W, SC	1:Full Duplex 0 :Half Duplex
		HW Rst		
		SW Rst		
7	Collision Test	Mode	R/W	Setting this bit to 1 will cause the COL pin to assert whenever the TX_EN pin is asserted. 1 = Enable COL signal test 0 = Disable COL signal test
		HW Rst	0	
		SW Rst	0	

Bit	Symbol	Type		Description
6	Speed Selection (MSB)	Mode	R/W	See bit 0.13
		HW Rst	See Desc.	
		SW Rst		
5:0	Reserved	Mode	RO	Will always be 00000.
		HW Rst	000000	
		SW Rst	00000	

3.10.2 Status Register

Address Offset: 0x01, or 0d01

Table 3-367, "Status Register," on page 346 summarizes the Register

Table 3-367. **Status Register**

Bit	Symbol	Type		Description
15	100Base-T4	Mode	RO	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
		HW Rst	Always 0	
		SW Rst	Always 0	
14	100BASE-X Full	Mode	RO	Capable of 100-Tx Full Duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
13	100BASE-X Half	Mode	RO	Capable of 100-Tx Half-Duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
12	10 Mbps Full-Duplex	Mode	RO	Capable of 10-Tx Full Duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
11	10 Mbps Half	Mode	RO	Capable of 10 Mbps Half Duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
10	100Base-T2 Full-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst	Always 0	
		SW Rst	Always 0	
9	100Base-T2 Half-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst	Always 0	
		SW Rst	Always 0	

Bit	Symbol	Type		Description
8	Extended Status	Mode	RO	Extended status information in register15
		HW Rst	Always 0	
		SW Rst	Always 0	
7	Reserved	Mode	RO	Always be 0.
		HW Rst	Always 0	
		SW Rst	Always 0	
6	MF Preamble Suppression	Mode	RO	PHY accepts management frames with preamble suppressed
		HW Rst	Always 1	
		SW Rst	Always 1	
5	Auto-negotiation Complete	Mode	RO	1: Auto negotiation process complete 0:Auto negotiation process not complete
		HW Rst	0	
		SW Rst	0	
4	Remote Fault	Mode	RO, LH	1: Remote fault condition detected 0:Remote fault condition not detected
		HW Rst	0	
		SW Rst	0	
3	Auto-negotiation Ability	Mode	RO	1 : PHY able to perform auto negotiation
		HW Rst	Always 1	
		SW Rst	Always 1	
2	Link Status	Mode	RO, LL	This register bit indicates whether the link was lost since the last read. For the current link status, read register bit 17.10 Link Real Time. 1 = Link is up 0 = Link is down
		HW Rst	0	
		SW Rst	0	
1	Jabber Detect	Mode	RO, LH	1: Jabber condition detected 0: Jabber condition not detected
		HW Rst	0	
		SW Rst	0	
0	Extended Capability	Mode	RO	1: Extended register capabilities
		HW Rst	Always 1	
		SW Rst	Always 1	

3.10.3 PHY Identifier

Address Offset: 0x02 or 0d02

Table 3-368, "PHY Identifier," on page 348 summarizes the Register

Table 3-368. **PHY Identifier**

Bit	Symbol	Type		Description
15:0	Organizationally Unique Identifer Bit 3:18	Mode	RO	Organizationally Unique Identifier bits 3:18
		HW Rst	Always 16'h004d	
		SW Rst	Always 16'h004d	

3.10.4 PHY Identifier 2

Address Offset: 0x03, or 0d03

Table 3-369, "PHY Identfier 2," on page 348 summarizes the Register

Table 3-369. **PHY Identfier 2**

Bit	Symbol	Type		Description
15	OUI LSB Model Number Revision Number	Mode	RO	Organizationally Unique Identifier bits 19:24
		HW Rst	Always 16'hd033	
		SW Rst	Always 16'hd033	

3.10.5 Auto-negotiation Advertisement Register

Address Offset: 0x04, or 0d04

Table 3-370, "Auto-negotiation Advertisement Register," on page 348 summarizes the Register.

Table 3-370. **Auto-negotiation Advertisement Register**

Bit	Symbol	Type		Description
15	Next Page	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed. 1 = Advertise 0 = Not advertised
		HW Rst	0	
		SW Rst	Update	

Bit	Symbol	Type		Description
14	Ack	Mode	RO	Must be 0
		HW Rst	Always 0	
		SW Rst	Always 0	
13	Remote Fault	Mode	R/W	1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
		HW Rst	Always 0	
		SW Rst	Always 0	
12	Reserved	Mode	RO	Always 0.
		HW Rst	Always 0	
		SW Rst	Always 0	
11	Asymmetric Pause	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause (this bit has added the pad control and can be set from the F001 top, its default value is one)
		HW Rst	1	
		SW Rst	Update	
10	PAUSE	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented (this bit has added the pad control and can be set from the F001 top, its default value is one)
		HW Rst	1	
		SW Rst	Update	
9	100Base-T4	Mode	RO	Not able to perform 100BASE-T4
		HW Rst	Always 0	
		SW Rst	Always 0	
8	100Base -TX	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	

Bit	Symbol	Type		Description
7	100BASE-TX Half Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
6	10BASE-TX Full Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
5	10BASE-TX Half Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
4:0	Selector Field	Mode	RO	Selector Field mode 00001 = 802.3
		HW Rst	Always 00001	
		SW Rst	Always 00001	

3.10.6 Link Partner Ability Register

Address Offset: 0x05, or 0d05

Table 3-371, "Link Partner Ability Register," on page 350 summarizes the Register

Table 3-371. **Link Partner Ability Register**

Bit	Symbol	Type		Description
15	Next Page	Mode	RO	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
		HW Rst	0	
		SW Rst	0	

Bit	Symbol	Type		Description
14	Ack	Mode	RO	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
		HW Rst	0	
		SW Rst	0	
13	Remote Fault	Mode	RO	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
		HW Rst	0	
		SW Rst	0	
12	Reserved	Mode	RO	Technology Ability Field Received Code Word Bit 12
		HW Rst	0	
		SW Rst	0	
11	Asymmetric Pause	Mode	RO	Technology Ability Field Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
		HW Rst	0	
		SW Rst	0	
10	PAUSE	Mode	RO	Technology Ability Field Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
		HW Rst	0	
		SW Rst	0	
9	100BASE-T4	Mode		Technology Ability Field Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
		HW Rst		
		SW Rst		
8	100BASE-TX Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
		HW Rst	0	
		SW Rst	0	
7	100BASE-TX Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
		HW Rst	0	
		SW Rst	0	
6	10BASE-TX Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
		HW Rst	0	
		SW Rst	0	

Bit	Symbol	Type		Description
5	10BASE-TX Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
		HW Rst	0	
		SW Rst	0	
4:0	Selector field	Mode	RO	Selector Field Received Code Word Bit 4:0
		HW Rst	00000	
		SW Rst	00000	

3.10.7 Auto-negotiation Expansion Register

Address Offset: 0x06, or 0d06

Table 3-372, "Auto-negotiation Expansion Register," on page 352 summarizes the Register

Table 3-372. **Auto-negotiation Expansion Register**

Bit	Symbol	Type		Description
15:5	Reserved	Mode	RO	Reserved. Must be 0.
		HW Rst	Always 0x000	
		SW Rst	Always 0x000	
4	Parallel Detection Fault	Mode	RO, LH	1: a fault has been detect 0: no fault has been detected
		HW Rst	0	
		SW Rst	0	
3	Link Partner Next Page Able	Mode	RO	1: Link partner is Next page able 0: Link partner is not next page able
		HW Rst	0	
		SW Rst	0	
2	Local Next Page Able	Mode	R/W	1 = Local Device is Next Page able
		HW Rst	1	
		SW Rst	1	
1	Page Received	Mode	RO, LH	1: A new page has been received 0: No new page has been received
		HW Rst	0	
		SW Rst	0	
0	Link Partner Auto-negotiation Able	Mode	RO	1: Link partner is auto negotiation able 0: Link partner is not auto negotiation able
		HW Rst	0	
		SW Rst	0	

3.10.8 Next Page Transmit Register

Address Offset: 0x07, or 0d07

Table 3-373, "Next Page Transmit Register," on page 353 summarizes the Register

Table 3-373. **Next Page Transmit Register**

Bit	Symbol	Type		Description
15	Next Page	Mode	R/W	Transmit Code Word Bit 15
		HW Rst	0	
		SW Rst	0	
14	Reserved	Mode	R/W	Transmit Code Word Bit 14
		HW Rst	0	
		SW Rst	0	
13	Message Page Mode	Mode	R/W	Transmit Code Word Bit 13
		HW Rst	0	
		SW Rst	0	
12	Ack	Mode	R/W	Transmit Code Word Bit 12
		HW Rst	0	
		SW Rst	0	
11	Toggle	Mode	RO	Transmit Code Word Bit 11
		HW Rst	0	
		SW Rst	0	
10:0	Message/ Unformatted Field	Mode	R/W	Transmit Code Word Bit 10:0
		HW Rst	0x001	
		SW Rst	0x001	

3.10.9 Link Partner Next Page Register

Address Offset: 0x08, or 0d08

Table 3-374, "Link Partner Next Page Register," on page 353 summarizes the Register

Table 3-374. **Link Partner Next Page Register**

Bit	Symbol	Type		Description
15	Next Page	Mode	RO	Received Code Word Bit 15
		HW Rst	0	
		SW Rst	0	
14	Reserved	Mode	RO	Received Code Word Bit 14
		HW Rst	0	
		SW Rst	0	

Bit	Symbol	Type		Description
13	Message Page Mode	Mode	RO	Received Code Word Bit 13
		HW Rst	0	
		SW Rst	0	
12	Ack2	Mode	RO	Received Code Word Bit 12
		HW Rst	0	
		SW Rst	0	
11	Toggle	Mode	RO	Received Code Word Bit 11
		HW Rst	0	
		SW Rst	0	
10:0	Message/ Unformatted Field	Mode	R/W	Received Code Word Bit 10:0
		HW Rst	0x000	
		SW Rst	0x000	

3.10.10 1000Base-T Control Register

Address Offset: 0x09, or 0d09

Table 3-375, "1000Base-T Control Register Register," on page 354 summarizes the Register

Table 3-375. **1000Base-T Control Register Register**

Bit	Symbol	Type		Description
15:13	Test Mode	Mode	R/W	TX_TCLK comes from the RX_CLK pin for jitter testing in test modes 2 and 3. After exiting the test mode, hardware reset or software reset (register 0.15) should be issued to ensure normal operation. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved
		HW Rst	000	
		SW Rst	Retain	
12	Master/Slave manual Configuration Enable	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration
		HW Rst	0	
		SW Rst	Update	

Bit	Symbol	Type		Description
11	Master/Slave Configuration	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down Register 9.11 is ignored if register 9.12 is equal to 0. 1 = Manual configure as MASTER 0 = Manual configure as SLAVE
		HW Rst	0	
		SW Rst	Update	
10	Port Type	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down Register 9.10 is ignored if register 9.12 is equal to 1. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
		HW Rst	0	
		SW Rst	Update	
9	1000Base-T Full Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
8	1000Base-T Half-Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised Note: the default setting is no 1000 baset/half duplex advertised
		HW Rst	0	
		SW Rst	Update	
7:0	Reserved	Mode	R/W	
		HW Rst	0	
		SW Rst	0	

3.10.11 1000Base-T Status Register

Address Offset: 0x0A, or 0d10

Table 3-376, "1000Base-T Status Register," on page 356 summarizes the Register

Table 3-376. **1000Base-T Status Register**

Bit	Symbol	Type		Description
15	Master/Slave Configuration Fault	Mode	RO, LH	This register bit will clear on read 1: Master/Slave configuration fault detected 0: No fault detected
		HW Rst	0	
		SW Rst	0	
14	Master/Slave Configuration Resolution	Mode	RO	This register bit is not valid until register 6.1 is 1. 1: Local PHY cnfiguration resolved to Master 0: Local PHY cnfiguration resolved to Slave
		HW Rst	0	
		SW Rst	0	
13	Local Receiver Status	Mode	RO	1:Local Receiver OK 0:Local Receiver Not OK
		HW Rst	0	
		SW Rst	0	
12	Remote Receiver Status	Mode	RO	1:Remote Receiver OK 0:Remote Receiver Not OK
		HW Rst	0	
		SW Rst	0	
11	Link Partner 1000Base-T Full Duplex Capability	Mode	RO	This register bit is not valid until register 6.1 is 1. 1: Link Partner is capable of 1000Base-T half duplex 0: Link Partner is not capable of 1000Base-T half duplex
		HW Rst	0	
		SW Rst	0	
10	Link Partner 1000Base-T Half Duplex Capability	Mode	RO	This register bit is not valid until register 6.1 is 1. 1: Link Partner is capable of 1000Base-T full duplex 0: Link Partner is not capable of 1000Base-T full duplex
		HW Rst	0	
		SW Rst	0	
9:8	Reserved	Mode	RO	
		HW Rst	Always 0	
		SW Rst	Always 0	
7:0	Idle Error Count	Mode	RO, SC	MSB of Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.
		HW Rst	0	
		SW Rst	0	

3.10.12 MMD Access Control Register

Address Offset: 0x0D, or 0d13

Table 3-377, "MMD Access Control Register," on page 357 summarizes the Register

Table 3-377. **MMD Access Control Register**

Bit	Symbol	Type		Description
15:14	Function	Mode	R/W	00=address 01=data,no post increment 10=data,post increment on reads and writes 11=data,post increment on writes only;
		HW Rst.	00	
		SW Rst.	Retain	
13:5	Reserved	Mode	R/O	
		HW Rst.	0	
		SW Rst.	0	
4:0	DEVAD	Mode	R/W	Device address
		HW Rst.	0	
		SW Rst.	Update	

3.10.13 MMD Access Address Data Register

Address Offset: 0x0E, or 0d14

Table 3-378, "MMD Access Address Data Register," on page 357 summarizes the Register

Table 3-378. **MMD Access Address Data Register**

Bit	Symbol	Type		Description
15:0	Address Data	Mode	R/W	If register13.15:14=00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register
		HW Rst.	00	
		SW Rst.	Retain	

3.10.14 Extended Status Register

Address Offset: 0x0F, or 0d15

Table 3-379, "Extended Status Register," on page 357 summarizes the Registers

Table 3-379. **Extended Status Register**

Bit	Symbol	Type		Description
15	1000BASE-X Full Duplex	Mode	RO	PHY not able to perform 1000BASE-X Full Duplex
		HW Rst	Always 0	
		SW Rst	Always 0	
14	1000BASE-X Half Duplex	Mode	RO	PHY not able to perform 1000BASE-X Half Duplex
		HW Rst	Always 0	
		SW Rst	Always 0	

Bit	Symbol	Type		Description
13	1000BASE-T Full-Duplex	Mode	RO	PHY able to perform 1000BASE-T Full Duplex
		HW Rst	Always 1	
		SW Rst	Always 1	
12	1000BASE-T Half-Duplex	Mode	RO	PHY not able to perform 1000BASE-T Half Duplex
		HW Rst	Always 0	
		SW Rst	Always 0	
11:0	Reserved	Mode	RO	
		HW Rst	Always 0	
		SW Rst	Always 0	

3.10.15 Function Control Register

Address Offset: 0x10, or 0d16

Table 3-380, "Function Control Register," on page 358 summarizes the Register

Table 3-380. **Function Control Register**

Bit	Symbol	Type		Description
15:12	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
11	Assert CRS on Transmit	Mode	R/W	This bit has effect only in 10Base-T half-duplex mode: 1 = assert on transmitting or receiving 0 = assert on reveiving. Do NOT assert on transmitting
		HW Rst	0	
		SW Rst	Retain	
10	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
9:8	Reserved	Mode	R/O	Always 0
		HW Rst	0	
		SW Rst	0	
6:5	MDI Crossover Mode	Mode	R/W	Changes to these bits are disruptive to the normal operation; therefore any changes to these registers must be followed by a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
		HW Rst	11	
		SW Rst	Updage	
4:3	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	

Bit	Symbol	Type		Description
2	SQE Test	Mode	R/W	SQE Test is automatically disabled in full-duplex mode. 1 = SQE test enabled 0 = SQE test disabled
		HW Rst	0	
		SW Rst	Retain	
1	Polarity Reversal	Mode	R/W	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled
		HW Rst	0	
		SW Rst	Retain	
0	Disable Jabber	Mode	R/W	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function
		HW Rst	0	
		SW Rst	Retain	

3.10.16 PHY Specific Status Register

Address Offset: 0x11, or 0d17

Table 3-381, "PHY Specific Status Register," on page 359 summarizes the Register

Table 3-381. **PHY Specific Status Register**

Bit	Symbol	Type		Description
15:14	Speed	Mode	RO	These status bits are valid when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
		HW Rst	00	
		SW Rst	Retain	
13	Duplex	Mode	RO	This status bit is valid only when Auto-Negotiation is complete or disabled. '1' = Full-Duplex '0' = Half-Duplex
		HW Rst	0	
		SW Rst	Retain	
12	Page Received (Real Time)	Mode	RO	1 = Page received 0 = Page not received
		HW Rst	0	
		SW Rst	Retain	
11	Speed and Duplex Resolved	Mode	RO	When Auto-Negotiation is not enabled for force speed mode. 1 = Resolved 0 = Not resolved
		HW Rst	0	
		SW Rst	0	
10	Link (Real Time)	Mode	RO	1 = Link up 0 = Link down
		HW Rst	0	
		SW Rst	0	
9:7	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	

Bit	Symbol	Type		Description
6	MDI Crossover Status	Mode	RO	This status bit is valid only when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = MDIX 0 = MDI
		HW Rst	0	
		SW Rst	Retain	
5	Wirespeed downgrade	Mode	RO	1 = Downgrade 0 = No Downgrade
		HW Rst	0	
		SW Rst	0	
4	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
3	Transmit Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disabled
		HW Rst	0	
		SW Rst	0	
2	Receive Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
		HW Rst	0	
		SW Rst	Retain	
1	Polarity (Real Time)	Mode	RO	1 = Reversed 0 = Normal
		HW Rst	0	
		SW Rst	0	
0	Jabber (Real Time)	Mode	RO	1 = Jabber 0 = No jabber
		HW Rst	0	
		SW Rst	Retain	

3.10.17 Interrupt Enable Register

Address Offset: 0x12, or 0d18

Table 3-382, "Interrupt Enable Register," on page 361 summarizes the Register

Table 3-382. **Interrupt Enable Register**

Bit	Symbol	Type		Description
15	Auto-Negotiation Error Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	

Bit	Symbol	Type		Description
14	Speed Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
13	Duplex Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
12	Page Received Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
11	Auto-Negotiation Completed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
10	Link Status Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
9	Symbol Error Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
8	False Carrier Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
7	FIFO Over/ Underflow Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
6	MDI Crossover Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
5	Wirespeed-downgrade Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
4	Energy Detect Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
3:2	Reserved	Mode	R/W	Always 00
		HW Rst	0	
		SW Rst	Retain	

Bit	Symbol	Type		Description
1	Polarity Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
0	Jabber Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	

3.10.18 Interrupt Status Register

Address Offset: 0x13, or 0d19

Table 3-383, "Interrupt Status Register," on page 362 summarizes the Register

Table 3-383. **Interrupt Status Register**

Bit	Symbol	Type		Description
15	Auto-Negotiation Error	Mode	RO, LH	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 1 = Auto-Negotiation Error 0 = No Auto-Negotiation Error
		HW Rst	0	
		SW Rst	Retain	
14	Speed Changed	Mode	RO, LH	1 = Speed changed 0 = Speed not changed
		HW Rst	0	
		SW Rst	Retain	
13	Reserved	Mode	RO, LH	Reserved
		HW Rst	0	
		SW Rst	Retain	
12	Page Received	Mode	RO	1 = Page received 0 = Page not received
		HW Rst	0	
		SW Rst	Retain	
11	Auto-Negotiation Completed	Mode	RO	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
		HW Rst	0	
		SW Rst	Retain	
10	Link Status Changed	Mode	RO, LH	1 = Link status changed 0 = Link status not changed
		HW Rst	0	
		SW Rst	Retain	
9	Symbol Error	Mode	RO, LH	1 = Symbol error 0 = No symbol error
		HW Rst	0	
		SW Rst	Retain	

Bit	Symbol	Type		Description
8	False Carrier	Mode	RO, LH	1 = False carrier 0 = No false carrier
		HW Rst	0	
		SW Rst	Retain	
7	FIFO Over/ Underflow	Mode	RO, LH	1 = Over/Underflow Error 0 = No FIFO Error Not implement, always 0.
		HW Rst	0	
		SW Rst	Retain	
6	MDI Crossover Changed	Mode	RO, LH	1 = Crossover changed 0 = Crossover not changed
		HW Rst	0	
		SW Rst	Retain	
5	Wirespeed-downgrade Interrupt	Mode	RO, LH	1 = Wirespeed-downgrade detected. 0 = No Wirespeed-downgrade.
		HW Rst	0	
		SW Rst	Retain	
4	Energy Detect Changed	Mode	RO, LH	1 = Energy Detect state changed 0 = No Energy Detect state change detected Not implement, always 0.
		HW Rst	0	
		SW Rst	Retain	
3:2	Reserved	Mode	RO, LH	Always 0
		HW Rst	0	
		SW Rst	Retain	
1	Polarity Changed	Mode	RO, LH	1 = Polarity Changed 0 = Polarity not changed
		HW Rst	0	
		SW Rst	Retain	
0	Jabber	Mode	RO, LH	1 = Jabber 0 = No jabber
		HW Rst	0	
		SW Rst	Retain	

3.10.19 Smart Speed Register

Address Offset: 0x14, or 0d20

Table 3-384, "Smart Speed Register," on page 364 summarizes the Register

Table 3-384. **Smart Speed Register**

Bit	Symbol	Type		Description
15:11	Reserved	Mode	RO	Reserved. must be 00000000
		HW Rst	0	
		SW Rst	0	

Bit	Symbol	Type		Description
10	aneg_now_qual	Mode	R/W	A rise of input pin "aneg_now" will set this bit to 1'b2, and cause PHY to restart auto-negotiation. Self-clear.
		HW Rst	1'b0	
		SW Rst	Retain	
9	Rev_aneg_qual	Mode	R/W	Make PHY to auto-negotiate in reversed mode. This bit takes its value from the input pin "rev_aneg" upon following: 1 HW reset(fall of rst_dsp_i); 2 PHY SW reset; 3 Rise of aneg_now.
		HW Rst	1'b0	
		SW Rst	Update	
8	Giga_dis_qual	Mode	R/W	Make PHY to disable GIGA mode. This bit takes its value from the input pin "giga_dis" upon following: 1 HW reset(fall of rst_dsp_i); 2 PHY SW reset; 3 Rise of aneg_now.
		HW Rst	1'b0	
		SW Rst	Update	
7	Cfg_pad_en	Mode	RO, LH	The default value is zero; if this bit is set to one, then the auto negotiation Arbitration FSM will bypass the LINK_STATUS_CHECK state when the 10 baset/100 baset ready signal is asserted.
		HW Rst	0	
		SW Rst	Retain	
6	Mr_ltdis	Mode	R/W	The default value is zero; if this bit is set to one, then the NLP Receive Link Integrity Test FSM will stays at the NLP_TEST_PASS state.
		HW Rst	0	
		SW Rst	Update	
5	Smartspeed_en	Mode	R/W	The default value is one; if this bit is set to one and cable inhibits completion of the training phase, then After a few failed attempts, the DSP PHY automatically downgrades the highest ability to the next lower speed: from 1000 to 100 to 10.
		HW Rst	1	
		SW Rst	Update	
4:2	Smartspeed_retry_limit	Mode	R/W	The default value is three; if these bits are set to three, then the DSP PHY will attempt five times before downgrading; The number of attempts can be changed through setting these bits.
		HW Rst	011	
		SW Rst	Update	
1	Bypass_smartspeed_timer	Mode	R/W	The default value is zero; if this bit is set to one, the Smartspeed FSM will bypass the timer used for stablility.
		HW Rst	0	
		SW Rst	Update	
0	Reserved	Mode	RO	Reserved. Must be 0.
		HW Rst	0	
		SW Rst	0	

3.10.20 Receive Error Counter Register

Address Offset: 0x15, or 0d21

Table 3-385, "Status Register," on page 365 summarizes the Register

Table 3-385. **Status Register**

Bit	Symbol	Type		Description
15:0	Receive Error Count	Mode	RO	Counter will peg at 0xFFFF and will not roll over. (when rx_dv is valid, count rx_er numbers) (in this version, only for 100Base-T and 1000Base-T)
		HW Rst	0x0000	
		SW Rst	Retain	

3.10.21 Virtual Cable Tester Control Register

Address Offset: 0x16, or 0d22

Table 3-386, "Virtual Cable Tester Contol Register," on page 365 summarizes the Register

Table 3-386. **Virtual Cable Tester Contol Register**

Bit	Symbol	Type		Description
15:10	Reserved	Mode	RO	Reserved
		HW Rst	Always 0	
		SW Rst	Always 0	
9:8	MDI Pair Select	Mode	R/W	Virtual Cable Tester™ Control registers. Use the Virtual Cable Tester Control Registers to select which MDI pair is shown in the Virtual Cable Tester Status register. 00 = MDI[0] pair 01 = MDI[1] pair 10 = MDI[2] pair 11 = MDI[3] pair
		HW Rst	00	
		SW Rst	Retain	
7:1	Reserved	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
0	Enable Test	Mode	R/W	When set, hardware automatically disable this bit when VCT is done. 1 = Enable VCT Test 0 = Disable VCT Test
		HW Rst	0	
		SW Rst	Retain	

3.10.22 Virtual Cable Tester Status Register

Address Offset: 0x1C, or 0d28

Table 3-387, "Virtual Cable Tester Status Register," on page 366 summarizes the Register

Table 3-387. **Virtual Cable Tester Status Register**

Bit	Symbol	Type		Description
15:10	Reserved	Mode	RO	Reserved.
		HW Rst	Always 0	
		SW Rst	Always 0	
9:8	Status	Mode	RO	The content of the Virtual Cable Tester Status Registers applies to the cable pair selected in the Virtual Cable Tester™ Control Registers. 11 = linkup state, no open or short in cable. 00 = Valid test, normal cable (no short or open in cable) 10 = Valid test, open in cable for MDI pair 0/2. Short in cable for MDI pair 1/3 01 = Valid test, short in cable for MDI pair 0/2. Open in cable for MDI pair 1/3
		HW Rst	00	
		SW Rst	00	
7:0	Delta_Time	Mode	R/W	Delta time to indicate distance. Length = Delta_Time * 0.824
		HW Rst	0	
		SW Rst	0	

3.10.23 Debug Port

Address Offset: 0x1D, or 0d29

Table 3-388, "Debug Port (Address Offset)," on page 366 summarizes the Register

Table 3-388. **Debug Port (Address Offset)**

Bit	Symbol	Type		Description
15:6	Reserved	Mode	RO	
		HW Rst	0	
		SW Rst	0	
5:0	Address Offset	Mode	R/W	The address index of the register will be write or read.
		HW Rst	0	
		SW Rst	0	

3.10.24 Debug Port 2 (R/W Port)

Address Offset: 0x1E, or 0d30

Table 3-389, "Debug Port 2 (R/W Port)," on page 367 summarizes the Register

Table 3-389. **Debug Port 2 (R/W Port)**

Bit	Symbol	Type		Description
15:0	Debug Data Port	Mode	R/W	The data port of debug register. Before access this register, must set the address offset first.
		HW Rst	0	
		SW Rst	0	

3.10.25 Debug Register — Analog Test Control

Address Offset: 0x00, or 0d00

Table 3-390 summarizes the Register

Table 3-390. **Debug Register — Analog Test Control**

Bit	Symbol	Type		Description
15	SEL_CLK125M_DSP	Mode	R/W	Control bit for RGMII interface Rx clock delay: 1 = RGMII Rx clock delay enable 0 = RGMII Rx clock delay disable
		HW Rst	1	
		SW Rst	0	
14:12	RESERVED	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
11	RESERVED	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	
10	RESERVED	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
9	RESERVED	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
8	RESERVED	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
7:5	RESERVED	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
4:3	RESERVED	Mode	R/W	Reserved
		HW Rst	2'h1	
		SW Rst	Retain	

Bit	Symbol	Type		Description
2	MANU_SWITCH_ON	Mode	R/W	DAC amplitude adjustment 1 = add +6% 0 = no increase
		HW Rst	1	
		SW Rst	Retain	
1	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
0	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	

3.10.26 Debug Register — System Mode Control

Address Offset: 0x03

Table 3-391. **Debug Register — System Mode Control**

Bit	Symbol	Type		Description
15	RESERVED	Mode	R/W	0
		HW Rst	0	
		SW Rst	0	
14	RESERVED	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
13:9	RESERVED	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	0	
8	OUT_MDIO_SW	Mode	R/W	Control the MDIO signal when POWER_DOWN mode is high 1 = MDIO is 1 0 = MDIO is valid, driven by inner state
		HW Rst	1	
		SW Rst	Retain	
7:4	RESERVED	Mode	R/W	Reserved
		HW Rst	4'b1111	
		SW Rst	Retain	
3:0	RESERVED	Mode	R/W	Reserved
		HW Rst	4'b1111	
		SW Rst	Retain	
7:5	RESERVED	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	

Table 3-391. **Debug Register — System Mode Control**

Bit	Symbol	Type		Description
4:3	RESERVED	Mode	R/W	Reserved
		HW Rst	2'h1	
		SW Rst	Retain	
2	MANU_SWITCH_ON	Mode	R/W	DAC amplitude adjustment 1 = add +6% 0 = no increase
		HW Rst	1	
		SW Rst	Retain	
1	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
0	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	

3.10.27 Debug Register — System Mode Control

Address Offset: 0x05, or 0d05

Table 3-392, "Debug Register — System Control Mode," on page 369 summarizes the Register

Table 3-392. **Debug Register — System Control Mode**

Bit	Symbol	Type		Description
15	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
14	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
13	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
12	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
11	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	

Bit	Symbol	Type		Description
10	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
9	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
8	Gtxclk_delay	Mode	R/W	Rgmii tx clock delay control bit: 1 = rgmii tx clock delay enable 0 = rgmii tx clock delay disable.
		HW Rst	0	
		SW Rst	Retain	
7	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
6	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
5:4	RES	Mode	R/W	Reserved
		HW Rst	2'b00	
		SW Rst	Retain	
3	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
2	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
1	100_ClassA	Mode	R/W	This bit is 100BT ClassA and ClassAB mode select bit. 0: 100BT ClassAB; 1: 100BT ClassA;
		HW Rst	1	
		SW Rst	Retain	
0	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	

3.10.28 Debug Register—Hib Control and Auto Negotiation Test Register

Address Offset: 0x0B

Table 3-393. **Hib Control and Auto Negotiation Test Register**

Bit	Symbol	Type		Description
15	PS_HIB_EN	Mode	R/W	Power hibernation control bit 1 = hibernation enable 0 = hibernation disable
		HW Rst	1	
		SW Rst	Retain	
14	WAKE_MODE	Mode	R/W	1 = PHY wakes up by energy detect or wake-up pin 0 = PHY wakes up only by energy detect
		HW Rst	0	
		SW Rst	Retain	
13	EN_ANY_CHANGE	Mode	R/W	1 = Turn on/off analog end at the same time 0 = Turn on/off analog end step by step
		HW Rst	1	
		SW Rst	Retain	
12	HIB_PULSE_SW	Mode	R/W	1 = PHY sends NLP pulse and detects signal from cables at hibernation state 0 = PHY does not send NLP pulse but detects signal from cables at hibernation state
		HW Rst	1	
		SW Rst	Retain	
11	GATE_25M_EN_SW	Mode	R/W	Always 1. 1 = Shut down the 25 MHz clock of auto negotiation at hibernation state 0 = The 25 MHz clock of auto negotiation is not controlled by hibernation
		HW Rst	1	
		SW Rst	1	
10	SEL_RST_80U	Mode	R/W	Duration of the reset triggered by speed mode change 1 = 80/120/160/240 µs (see bit 9:8 of this register) 0 = 240 µs
		HW Rst	1	
		SW Rst	Retain	
9:8	SEL_RST_TIMER	Mode	R/W	Duration configuration for reset timer 00 = 80 µs 01 = 120 µs 10 = 160 µs 11 = 240 µs
		HW Rst	00	
		SW Rst	Retain	
7	RESERVED	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
6:5	GTX_DLY_VAL	Mode	R/W	GTx clock delay select
		HW Rst	10	
		SW Rst	Retain	
4	BYPASS_BREAK_LINK_TIMER	Mode	R/W	1 = BREAL_LINK timer is bypassed when auto negotiation is restarted, thus auto negotiation state stays at TRANSMIT_DISABLE for one cycle (40 ns) 0 = Auto negotiation state stays at TRANSMIT_DISABLE for about 1.2 second when auto negotiation is restarted
		HW Rst	0	
		SW Rst	Retain	

Table 3-393. **Hib Control and Auto Negotiation Test Register**

Bit	Symbol	Type		Description
3	DBG_LINK_OK_100T	Mode	R/W	For link management use. The forced LINK_OK_100BT
		HW Rst	0	
		SW Rst	0	
2	DBG_LINK_OK_1000T	Mode	R/W	For link management use. The forced LINK_OK_1000BT
		HW Rst	0	
		SW Rst	0	
1	DBG_LINK_RDY_100T	Mode	R/W	For link management use. The forced LINK_RDY_100BT
		HW Rst	0	
		SW Rst	0	
0	DBG_EN_EN	Mode	R/W	For link management use. When this bit is set, the test bits in this register take effect.
		HW Rst	0	
		SW Rst	0	

3.10.29 Debug Register — RGMII Mode Selection

Address Offset: 0x012, or 0d18

Table 3-394 summarizes the Register

Table 3-394. **Debug Register — RGMII Mode Selection**

Bit	Symbol	Type		Description
15:14	RES	Mode	R/W	Reserved
		HW Rst	01	
		SW Rst	Retain	
13:12	RES	Mode	R/W	Reserved
		HW Rst	00	
		SW Rst	Retain	
11	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
10	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
9:6	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	

Bit	Symbol	Type		Description
5	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	
4	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
3	Rgmii_mode	Mode	R/W	1: select RGMII interface with MAC; 0: select GMII/MII interface with MAC.
		HW Rst	0	
		SW Rst	Retain	
2	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	1	
1:0	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	

3.10.30 Debug Register—Green Feature Configure Register

Address offset: 0x3D

Table 3-395.

Bit	Symbol	Type		Description
15	RESERVED	Mode	R/W	
		HW Rst	0	
		SW Rst	Retain	
14	REVERSE			
13:8	RESERVED	Mode	R/W	
		HW Rst	6'h28	
		SW Rst	Retain	
7	RESERVED	Mode	R/W	
		HW Rst	1	
		SW Rst	Retain	
6	GATE_CLK_IN1000	Mode	R/W	0 = When in 1000BT mode, gate dig100/dig10/vct clk 1 = When in 1000BT mode, do not gate dig100/dig10/vct clk
		HW Rst	1	
		SW Rst	Retain	

Table 3-395.

Bit	Symbol	Type		Description
5:0	RESERVED	Mode	R/W	
		HW Rst	6'h20	
		SW Rst	Retain	

3.11 MMD3 — PCS Register

3.11.1 PCS Control1

Address Offset: 0x00, or 0d00

Device Address = 3

Table 3-396, "PCS Control1," on page 374 summarizes the Register

Table 3-396. **PCS Control1**

Bit	Symbol	Type		Description
15	Pcs_rst	Mode	R/W	Reset bit, self clear. When write this bit 1 : 1, reset the registers(not vender specific) in MMD3/MMD7. 2, cause software reset in mii register0 bit15.
		HW Rst	0	
		SW Rst	0	
14:11	Reserved	Mode	R/O	Always 0
		HW Rst	0	
		SW Rst	0	
10	Clock_stoppable	Mode	R/W	Not Implemented
		HW Rst	1	
		SW Rst	Retain	
9:0	Reserved	Mode	R/W	Always 0
		HW Rst	1	
		SW Rst	Retain	

3.11.2 PCS Status1

Address Offset: 0x01, or 0d01

Device Address = 3

Table 3-396, "PCS Control1," on page 374 summarizes the Register

Table 3-397. **PCS Control1**

Bit	Symbol	Type		Description
15:12	Reserved	Mode	R/W	Always 0.
		HW Rst	0	
		SW Rst	0	
11	Tx lp idle received	Mode	R/O	When read as 1, it indicates that the transmit PCS has received low power idle signaling one or more times since the register was last read. Lach High.
		HW Rst	0	
		SW Rst	0	
10	Rx lp idle received	Mode	R/W	When read as 1, it indicates that the recive PCS has received low power idle signaling one or more times since the register was last read. Lach High.
		HW Rst	0	
		SW Rst	0	
9	Tx lp idle indication	Mode	R/W	When read as 1, it indicates that the transmit PCS is currently receiving low power idle signals.
		HW Rst	0	
		SW Rst	0	
8	Rx lp idle indication	Mode	R/W	When read as 1, it indicates that the receive PCS is currently receiving low power idle signals.
		HW Rst	0	
		SW Rst	0	
7:0	Reserved	Mode	R/O	Always 0
		HW Rst	0	
		SW Rst	0	

3.12 EEE Capability Register

Address Offset: 0x014, or 0d020

Device Address = 3

Table 3-398, "EEE Capability Register," on page 376 summarizes the Register

Table 3-398. **EEE Capability Register**

Bit	Symbol	Type		Description
15:3	Reserved	Mode	R/O	Always 0.
		HW Rst	0	
		SW Rst	0	
2	1000BT EEE	Mode	R/O	EEE is supported for 1000Base-T.
		HW Rst	1	
		SW Rst	1	
1	100BT EEE	Mode	R/O	EEE is supported for 100Base-T.
		HW Rst	1	
		SW Rst	1	
0	Reserved	Mode	R/W	Always 0.
		HW Rst	0	
		SW Rst	0	

3.12.1 EEE Wake Error Counter

Address Offset: 0x016, or 0d022

Device Address = 3

Table 3-399 summarizes the Register

Table 3-399. **EEE Wake Error Counter**

Bit	Symbol	Type		Description
15:0	EEE wake error counter	Mode	R/O	Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. This counter is clear after read, and hold at all ones in the case of overflow.
		HW Rst	0	
		SW Rst	0	

3.13 MMD7 — Auto-negotiation Register

Address Offset: 0x0, or 0d0

Device Address = 7

Table 3-400, "AN Control1," on page 377 summarizes the Register

Table 3-400. **AN Control1**

Bit	Symbol	Type		Description
15	an_rst	Mode	R/O	Reset bit, self clear. When write this bit 1 : 1, reset the registers(not vender specific) in MMD3/MMD7. 2, cause software reset in mii register0 bit15.
		HW Rst	0	
		SW Rst	0	
14	Reserved	Mode	R/O	Always 0.
		HW Rst	1	
		SW Rst	1	
13	Xnp_ctrl	Mode	R/O	If mii register4 bit12 is set to 0, setting of this bit shall have no effect. 1 = Local device intends to enable the exchange of extended next page; 0 = Local device does not intend to enable the exchange of extended next page;
		HW Rst	1	
		SW Rst	1	
12:0	Reserved	Mode	R/W	Always 0.
		HW Rst	0	
		SW Rst	0	

3.13.1 AN Package

Address Offset: 0x05, or 0d05

Device Address = 7

Table 3-401, "AN Package," on page 377 summarizes the Register

Table 3-401. **AN Package**

Bit	Symbol	Type		Description
15:8	Reserved	Mode	R/O	Always 0.
		HW Rst	0	
		SW Rst	0	
7	auto_neg_present	Mode	R/O	Always 1
		HW Rst	1	
		SW Rst	1	

Bit	Symbol	Type		Description
6:4	Reserved	Mode	R/O	Always 0
		HW Rst	0	
		SW Rst	0	
3	PCS present	Mode	R/O	Always 1
		HW Rst	1	
		SW Rst	1	
2:1	Reserved	Mode	R/W	Always 0
		HW Rst	0	
		SW Rst	0	
0	mii_reg_present	Mode	R/W	Always 1
		HW Rst	1	
		SW Rst	1	

3.13.2 AN Status

Address Offset: 0x01, or 0d1

Device Address = 7

Table 3-402 summarizes the Register

Table 3-402. **AN Package**

Bit	Symbol	Type		Description
15	Reserved	Mode	R/O	
		HW Rst	0	
		SW Rst	0	
14	Reserved Xnp_status	Mode	R/O	1 = both Local device and link partner have indicated support for extended next page; 0 = extended next page shall not be used.
		HW Rst	0	
		SW Rst	0	
6:13	xnp_ctrl	Mode	R/O	
		HW Rst	0	
		SW Rst	0	
12:0	Reserved	Mode	R/O	
		HW Rst	0	
		SW Rst	0	

3.13.3 AN XNP Transmit

Address Offset: 0x016, or 0d22

Device Address = 7

Table 3-403 summarizes the Register

Table 3-403. **AN XNP Transmit**

Bit	Symbol	Type		Description
15:0	Xnp_22	Mode	R/O	A write to this register set mr_next_page_loaded.
		HW Rst	0	
		SW Rst	0	

3.13.4 AN XNP Transmit1

Address Offset: 0x017, or 0d23

Device Address = 7

Table 3-404, "AN XNP Transmit1," on page 379 summarizes the Register

Table 3-404. **AN XNP Transmit1**

Bit	Symbol	Type		Description
15:0	Xnp_23	Mode	R/O	
		HW Rst	0	
		SW Rst	0	

3.13.5 AN XNP Transmit2

Address Offset: 0x018, or 0d24

Device Address = 7

Table 3-405, "AN XNP Transmit2," on page 379 summarizes the Register

Table 3-405. **AN XNP Transmit2**

Bit	Symbol	Type		Description
15:0	Xnp_23	Mode	R/O	
		HW Rst	0	
		SW Rst	0	

3.13.6 AN LP XNP Ability

Address Offset: 0x019, or 0d25

Device Address = 7

Table 3-406, "AN LP XNP Ability," on page 380 summarizes the Register

Table 3-406. **AN LP XNP Ability**

Bit	Symbol	Type		Description
15:0	Xnp_23	Mode	R/O	
		HW Rst	15'h0	
		SW Rst	15'h0	

3.13.7 AN LP XNP Ability1

Address Offset: 0x01A, or 0d26

Device Address = 7

Table 3-407, "AN LP XNP Ability1," on page 380 summarizes the Register

Table 3-407. **AN LP XNP Ability1**

Bit	Symbol	Type		Description
15:0	Lp_xnp_2	Mode	R/O	Latched when lp_xnp_1 is read
		HW Rst	15'h0	
		SW Rst	15'h0	

3.13.8 AN LP XNP Ability2

Address Offset: 0x01B, or 0d27

Device Address = 7

Table 3-408 summarizes the Register

Table 3-408. **AN LP XNP Ability2**

Bit	Symbol	Type		Description
15:0	Lp_xnp_3	Mode	R/O	Latched when lp_xnp_1 is read
		HW Rst	15'h0	
		SW Rst	15'h0	

3.13.9 EEE Advertisement

Address Offset: 0x3C (Hex)

Device Address = 7

Table , "," on page 381 summarizes the Register

Table 3-409. **EEE Advertisement**

Bit	Symbol	Type		Description
15:3	Reserved	Mode	R/O	Always 0.
		HW Rst	0	
		SW Rst	0	
2	EEE_1000BT	Mode	R/W	If Local device supports EEE operation for 1000BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst	1'b1	
		SW Rst	Retain	
1	EEE_100BT	Mode	R/W	If Local device supports EEE operation for 100BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst	1'b1	
		SW Rst	Retain	
0	Reserved	Mode	R/O	Always 0.
		HW Rst	0	
		SW Rst	0	

3.13.10 EEE LP Advertisement

Address Offset: 0x3D (Hex)

Device Address = 7

Table 3-410 summarizes the Register

Table 3-410. **EEE LP Advertisement**

Bit	Symbol	Type		Description
15:3	Reserved	Mode	R/O	Always 0.
		HW Rst	0	
		SW Rst	0	
2	EEE_1000BT	Mode	R/O	If Local device supports EEE operation for 1000BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst	0	
		SW Rst	0	
1	EEE_100BT	Mode	R/O	If Local device supports EEE operation for 100BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst	0	
		SW Rst	0	
0	Reserved	Mode	R/O	Always 0.
		HW Rst	0	
		SW Rst	0	

3.13.11 EEE Ability Auto-negotiation Result

Address Offset: 0x8000 (Hex)

Device Address = 7

Table 3-411 summarizes the Register

Table 3-411. **EEE LP Advertisement**

Bit	Symbol	Type		Description
15:3	Reserved	Mode	R/O	Always 0.
		HW Rst	0	
		SW Rst	0	
2	EEE_1000BT_en	Mode	R/O	1 = 1000BT az enable; both sides support EEE operation for 1000BT, and EEE operation is desired; 0 = 1000BT az disable; Either side does not support EEE operation for 1000BT, or EEE operation is not desired.
		HW Rst	0	
		SW Rst	0	
1	EEE_100BT_en	Mode	R/O	1 = 100BT az enable; both sides support EEE operation for 100BT, and EEE operation is desired; 0 = 100BT az disable; Either side does not support EEE operation for 100BT, or EEE operation is not desired.
		HW Rst	0	
		SW Rst	0	
0	Reserved	Mode	R/O	Always 0.
		HW Rst	0	
		SW Rst	0	

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 summarizes the absolute maximum ratings and Table 4-2 lists the recommended operating conditions for the AR8327. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 4-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max Rating	Unit
AVDD	1.1 V digital core supply voltage	1.6	V
VDD25_IO	2.5 V digital supply voltage	3.0	V
DVDD	1.1 V digital supply voltage	1.6	V
VDD33	Analog 3.3 V supply voltage	4.0	V
T_{store}	Storage temperature	–65 to 150	°C
ESD	Electrostatic discharge tolerance	2000	V

NOTE: For a 2-layer PCB design, we strongly recommend the use of external power — 1.1V for AVDD and DVDD. This will reduce thermal effects.

NOTE: For a four-layer PCB design, we strongly recommend the use of a reserve external power supply for AVDD and DVDD when using the internal switch regulator.

4.2 Recommended Operating Conditions

Table 4-2. **Recommended Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	3.3 V I/O voltage	3.0	3.3	3.6	V
VDD25_IO	2.5 V analog/digital	2.4	2.62	2.75	V
AVDD/DVDD	1.2 V analog/digital	1.15	1.2	1.26	V
$T_{ambient}$	Ambient Temperature		25		°C
T_J	Junction Temperature	0		120	°C
Ψ_{JT}	Thermal Dissipation Coefficient		2.5		°C/W

4.3 RGMII/GMII Characteristics

Table 4-3 shows the RGMII/GMII DC characteristics.

Table 4-3. **RGMII/GMII DC Characteristics**

Symbol	Parameter	Min	Max	Unit
V_{OH}	Output high voltage	2.2	—	V
V_{OL}	Output low voltage	—	0.4	V

Table 4-3. **RGMII/GMII DC Characteristics**

I_{IH}	Input high current	—	–0.4	mA
I_{IL}	Input low current	0.4	—	mA
VIH	Input high voltage	1.7	3.6	V
VIL	Input high voltage	—	0.7	V

4.4 Power-on Strapping

Table 4-4 shows the pin-to-PHY core configuration signal power-on strapping.

Table 4-4. **Power-On Strapping**

Pin Name	Pin Signal	Pin	Description	
Mode_oclk_selH	RXD1_0	A69	0	Controls the voltage output of switching regulator at LX. 0 for 1.1V
			1	Use external 1.1V power source, the external power source must be between 1.1V and 1.26V
AZ_EN	RXDV_1	A54	0	Disable 802.3az
			1	Enable 802.3az
MDIO_EN	SPI_DO	B44	0	UART interface
			1	MDIO interface
UART_SPEED	RXD0_0	A68	0	Normal operation
			1	High speed for function test
control_dac[1]	RX_D0_1	A55	0	power-saving mode — set in concert with pin A70, below 2'b00: Power-saving off 2'b01: Power-saving mode 1 2'b10: Power-saving mode 2 2'b11: Power-saving mode 3
control_dac[0]	RX_D2_0	A70	0	power-saving mode — set in concert with pin A55, above
SPI_SIZE	RXD2_1	B49	0	1K
				4K or 2K
FUNC_MODE0	SPI_CS	A52	00	Normal Operation
FUNC_MODE1	SPI_CLK	B45	01	Test Mode
			10	
			11	
LED_OPEN_EN	INT_n	B68	0	Driver
			1	Open Drain
SPI_EN	RXCLK_0	A65	0	No EEPROM connected
			1	EEPROM enable

4.4.12 Power-on-Reset Timing

Figure 4-2 shows the Power-on-Reset timing diagram.

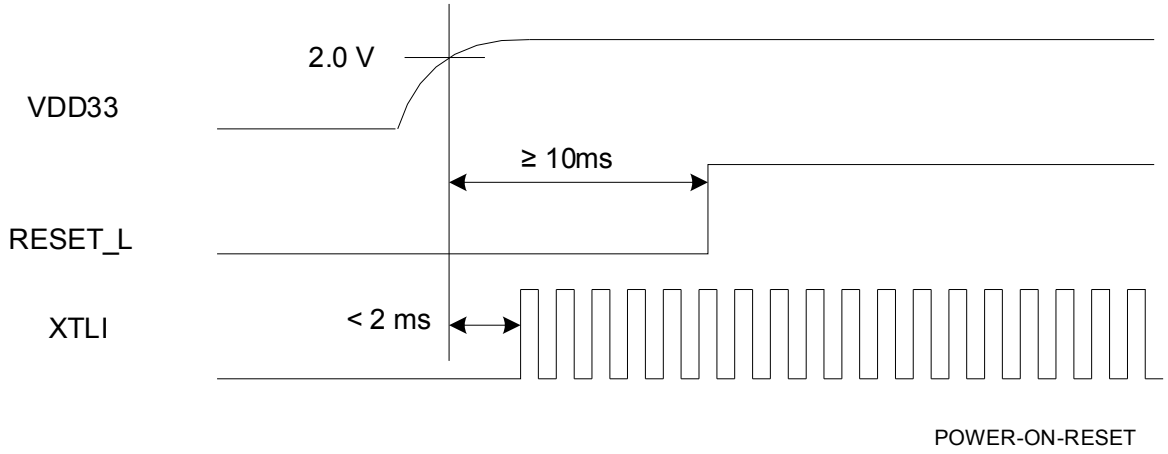

Figure 4-1. **Power-on-Reset Timing Diagram**

4.5 AC Timing

4.5.1 XTAL/OSC Timing

Figure 4-2 shows the XTAL timing diagram.

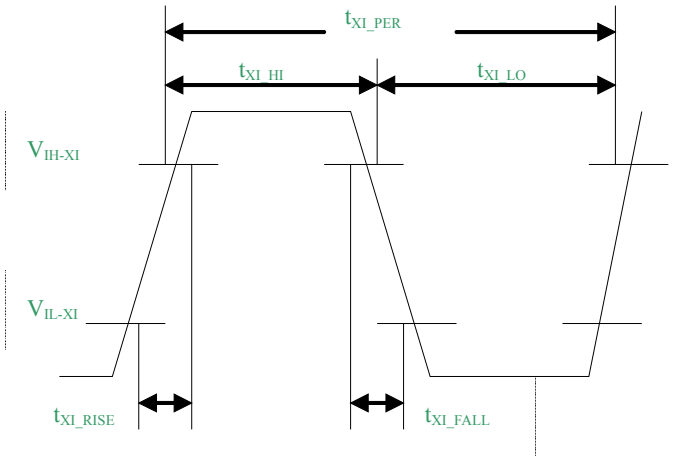

Figure 4-2. **XTAL/OSC Timing Diagram**

Table 4-5. **XTAL/OSC Timing**

Symbol	Parameter	Min	Typ	Max	Unit
T_XI_PER	XI/OSCI Clock Period	40.0 - 50ppm	40.0	40.0 + 50ppm	ns
T_XI_HI	XI/OSCI Clock High	14	20.0		ns
T_XI_LO	XI/OSCI Clock Low	14	20.0		ns
T_XI_RISE	XI/OSCI Clock Rise Time, V_{IL} (max) to V_{IH} (min)			4	ns
T_XI_FALL	XI/OSCI Clock Fall time, V_{IL} (max) to V_{IH} (min)			4	ns
V_IH_XI	The XTLI input high level	0.8		1.4	V
V_IL_XI	The xtli input low lever voltage	-0.3		0.15	V

4.5.2 MII Timing

Figure 4-3 shows the MII timing diagram.

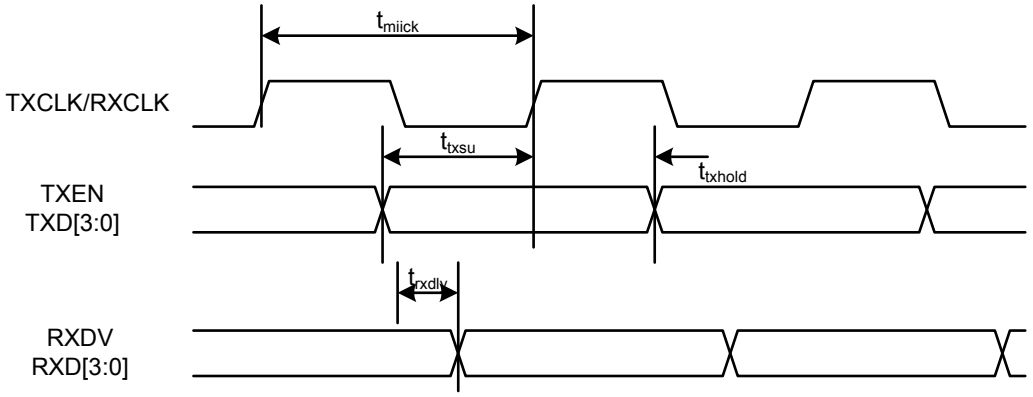

Figure 4-3. **100BASE-TX MII Input Timing Diagram**

Table 4-6. **MII Timing**

Symbol	Parameter	Min	Typ	Max	Unit
tmiick	TXCLK/RXCLK Period		40		ns
ttxsu	TXEN and TXD to TXCLK rising setup	10			ns
ttxhold	TXEN and TXD to TXCLK rising hold	10			ns
ttxdly	RXCLK falling to RXDV, and RXD Output Delay	0		8	ns

4.5.3 GMII Timing

Figure 4-4 shows the GMII timing diagram.

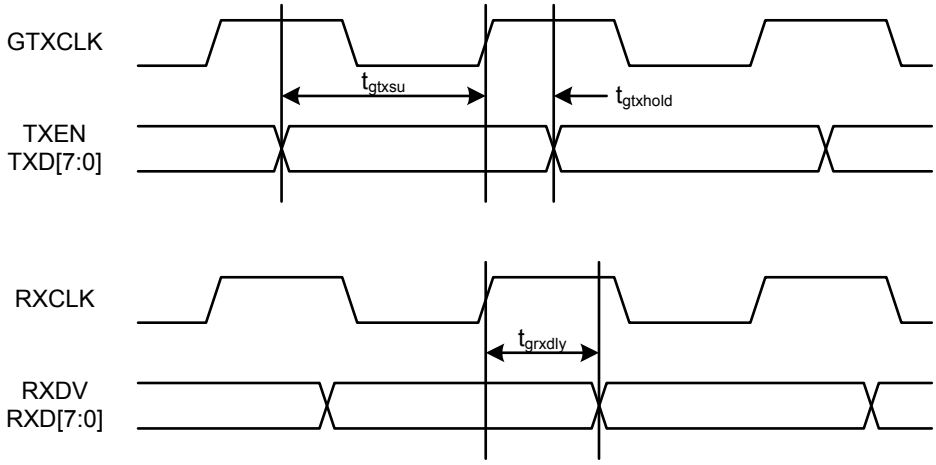

Figure 4-4. **1000Base-TX GMII Timing Diagram**

Table 4-7. **1000Base-Tx GMII Timing**

Symbol	Parameter	Min	Typ	Max	Unit
tgtxsu	TXEN and TXD to GTXCLK	2.0			ns
tgtxhold	TXEN and TXD GTXCLK rising hold time	0			ns
tgrxdly	RXCLK rising to RXDV, and RXD Output Delay	0.5		5.5	ns

4.5.4 *RGMII Timing*

Figure 4-5 shows the RGMII timing diagram.

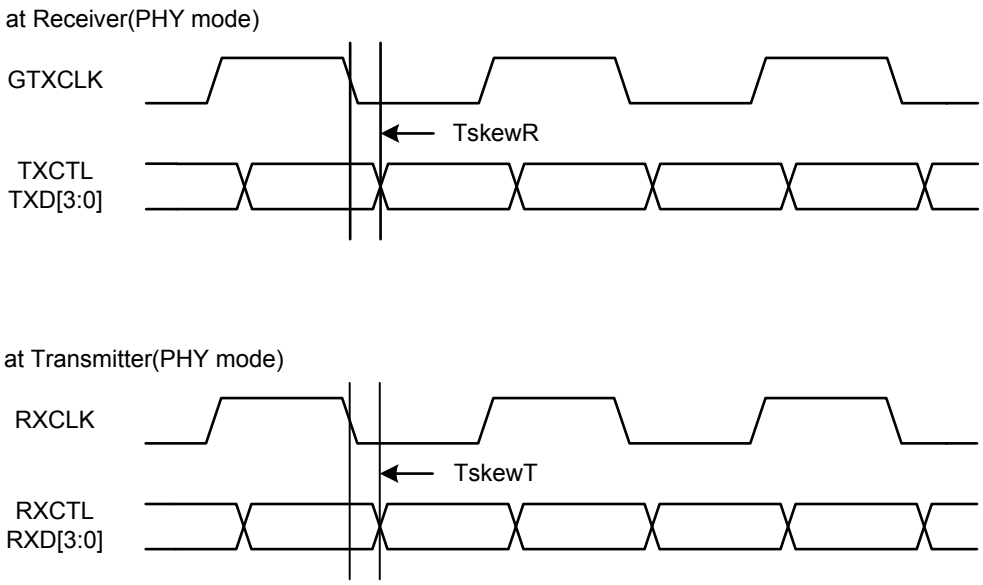

Figure 4-5. **RGMII Timing Diagram**

Table 4-8. **Reduced GMII Timing**

Symbol	Parameter	Min	Typ	Max	Unit
TskewT	Data to Clock output skew	-0.5		0.5	ns
TskewR	Data to Clock input skew	1		2.6	ns
	Data Input to Clock Edge	1			ns
	Hold Time	1			ns

4.5.5 SPI Timing

Figure 4-6 shows the SPI timing diagram.

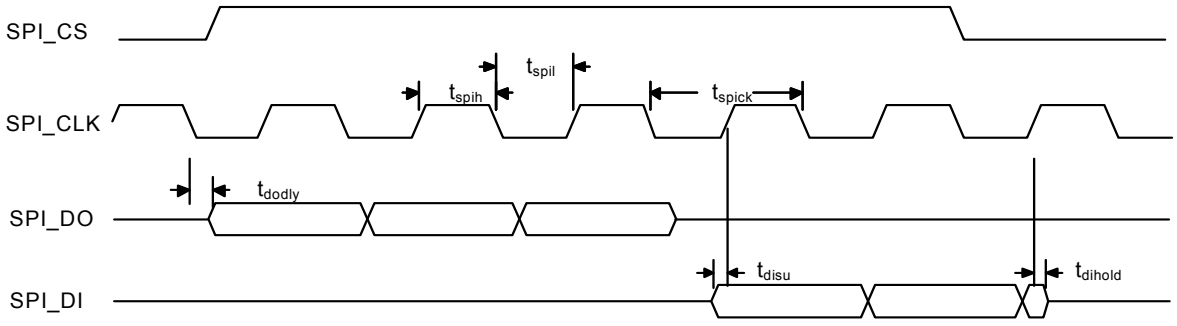

Figure 4-6. **EEPROM Interface Timing Diagram**

Table 4-9. **EEPROM Interface Timing**

Symbol	Parameter	Min	Typ	Max	Unit
tspick	SPI_CLK Period		TBD		ns
tspil	SPI_CLK Low Period	-		-	ns
tspih	SPI_CLK High Period	-		-	ns
tdisu	SPI_DI to SPI_CLK Rising Setup Time	10			ns
tdihold	SPI_DI to SPI_CLK Rising Hold Time	10			ns
tdodly	SPI_CLK Falling to SPI_DO Output Delay Time			20	ns

4.5.6 MDIO Timing

Figure 4-7 shows the MDIO timing diagram.

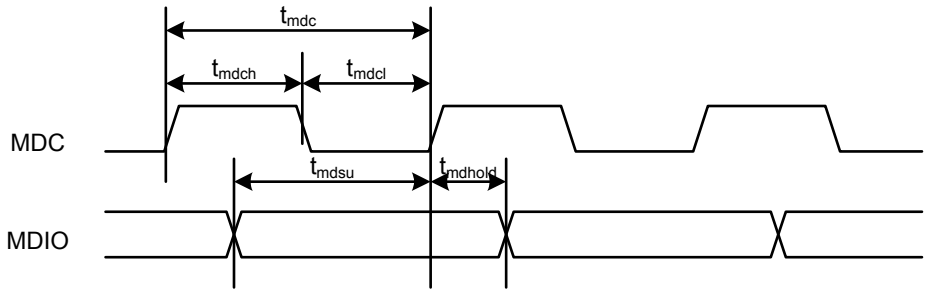

Figure 4-7. **MDIO Timing Diagram**

Table 4-10. **MDIO Timing**

Symbol	Parameter	Min	Typ	Max	Unit
tmdc	MDC Period	100			ns
tmdcl	MDC Low Period	40			ns
tmdch	MDC High Period	40			ns
tmdsu	MDIO to MDC rising setup time	10			ns
tmdhold	MDIO to MDC rising hold time	10			ns

4.6 Typical Power Consumption Parameters

The following conditions apply to the typical characteristics unless otherwise specified:

DVDD/AVDD = 1.1 V

VDD33 = 3.3V
Tamb = 25 °C

Table 4-11 shows the typical power drain on each of the on-chip power supply domains as a function of the AR8327's operating mode.

Table 4-11. **Total System Power (1000 Base-T)**

Link Type	Link Status	3.3V (mA)	1.1V (mA)	Power Consumption (mW)
	no link	30	81	188.1
1000M	All Ports Active	294	753	1798.5
	Two Ports Active	126	376	829.4
	Three Ports Active	185	520	1182.5
	Four Ports Active	244	627	1494.9
100M	All Ports Active	110	209	592.9
	Two Ports Active	58	129	333.3
	Three Ports Active	80	160	440
	Four Ports Active	94	182	510.4
1000M	All Ports 802.3az Enabled	114	—	376.2
100M	All Ports 802.3az Enabled	100	—	330

5. Package Dimensions

The AR8327 is packaged in a 148-pin DRQFN package. The body size is 12 mm by 12 mm. The package drawings and dimensions are provided in Figure 5-1 and Table 5-1.

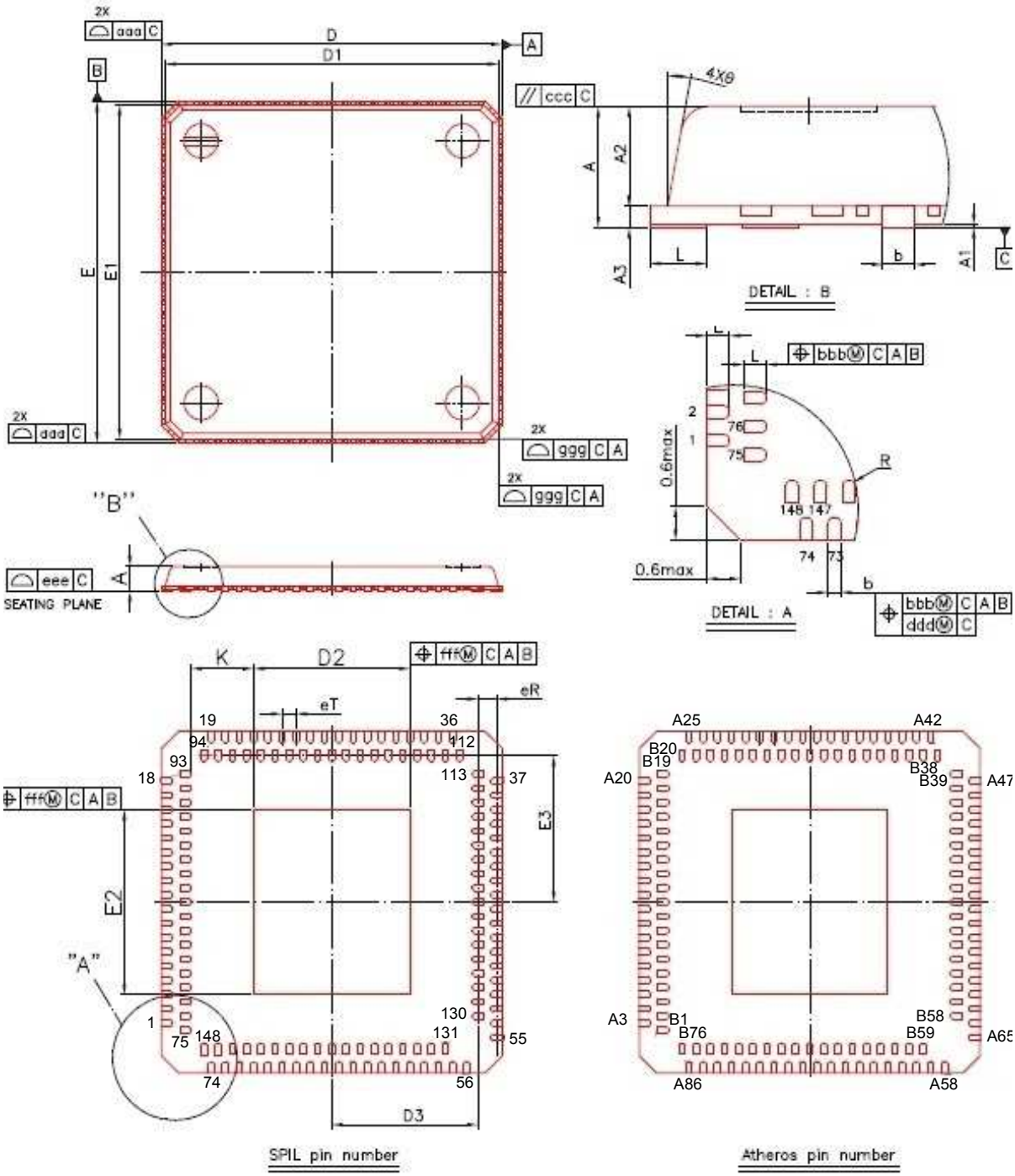

Figure 5-1. **148 pins DRQFN Package Drawing**

Table 5-1. **Package Dimensions (in mm)**

Symbol	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.65	0.70	0.75
A3		0.15 REF	
b	0.18	0.22	0.30
D/E	11.90	12.00	12.10
D1/E1		11.75 BSC	
D2	5.40	5.50	5.60
E2	6.40	6.50	6.60
D3/E3		5.15 BSC	
eT		0.50 BSC	
eR		0.65 BSC	
L	0.30	0.40	0.50
Theta	5	—	15
K	0.20	—	—
R	0.09	—	—
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
ggg		0.20	

6. Ordering Information

The ordering information is listed in Table 6-1.

Table 6-1. **Ordering Information**

Ordering Number	Package	Default Ordering Unit
AR8327-AL1A	DR-QFN 148(12 mm × 12 mm)	Tray
AR8327-AL1A-R	DR-QFN 148 (12 mm × 12 mm)	Tape and reel
AR8327N-AL1A	DR-QFN 148 (12 mm × 12 mm)	Tray
AR8327N-AL1A-R	DR-QFN 148 (12 mm × 12 mm)	Tape and reel

7. Top Side Marking

The top side marking is listed in Table 7-1.

Table 7-1. **Top Side Marking**

Ordering Number	Marking
AR8327-AL1A AR8327-AL1A-R	AR8327-AL1A
AR8327N-AL1A AR8327N-AL1A-R	AR8327N-AL1A

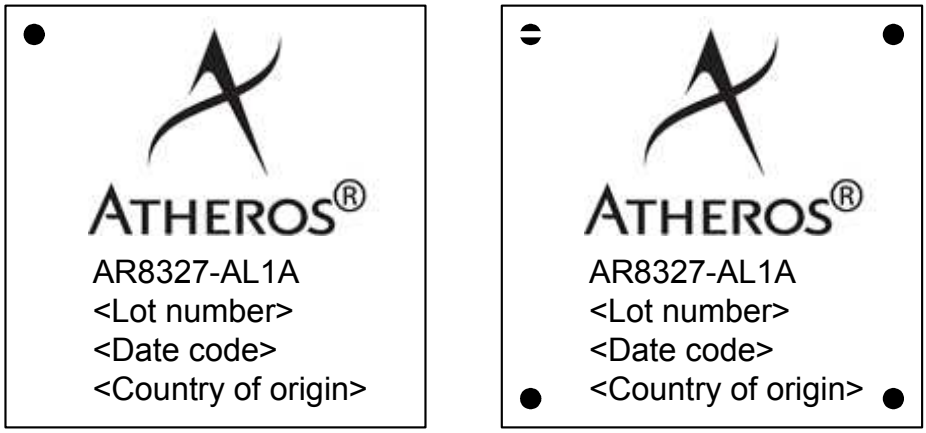

Figure 7-1. **Top Side Marking (AR8327)**

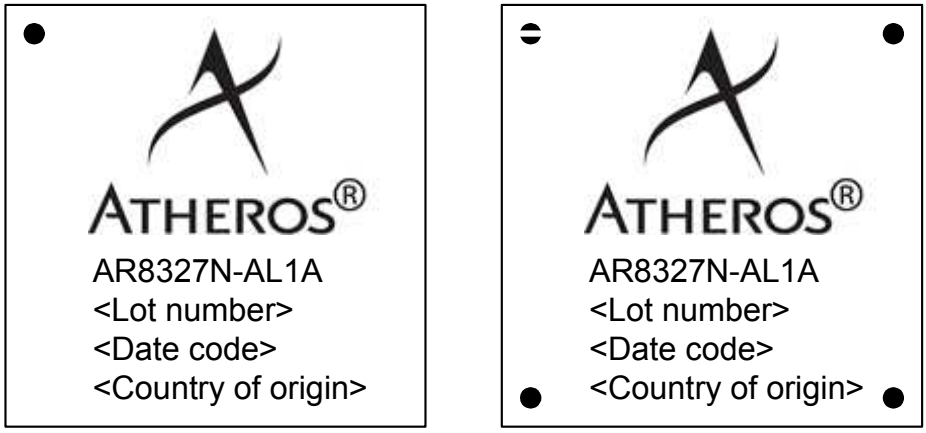

Figure 7-2. **Top Side Marking (AR8327N)**

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